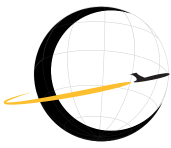


VIA QUALIFICATION REPORT

October 9, 2009

INTRODUCTION

This report describes the qualification of filled via substrates for use in space borne microelectronic circuits. The qualification described herein, is limited to filled via substrates as produced by Diablo Industries Minden, NV.

QUALIFICATION PLAN

Please refer to: Filled Via Qualification Plan dated July 29, 2009 (see Appendix A).

TEST RESULTS (Bare Substrate Test Samples)

Visual Inspection

All sample substrates comply with drawings A001 & B001 (see Appendix B), and Aerospace Electronics process specification AE-XXXX Acceptance Criteria for Metallized Substrates.

Film Adhesion Tests

All sample substrates passed adhesion tape test.

Thermal Shock

All filled via substrates passed thermal shock tests. High magnification inspection was performed after each 5 cycle interval and compared to pre cycle photos. Post cycle photos were taken for pre/post shock comparisons (see Appendix C).

One control sample (unfilled vias) showed indications of via metal separation.

Electrical Resistance

All filled via substrates passed electrical resistance tests. Test results ± .01 ohm:

Filled via .34 ohm (resistance between housing & via pad)
Unfilled via .41 ohm (resistance between housing & via pad
Reference .30 ohm (resistance across housing, i.e.. metal-to-metal)

TEST RESULTS (Functional Circuit Test Samples)

Thermal Cycle

Both functional amplifiers (SN 001 & SN 002) passed non-operating thermal cycle tests. This was verified by an operating thermal cycle test in which RF performance was continuously monitored (see Appendix D).

CONCLUSION

Filled via substrates as produced by Diablo Industries are qualified for use in space borne microelectronic circuits.

APPENDIX A

FILLED VIA QUALIFICATION PLAN

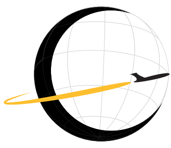
FILLED VIA QUALIFICATION PLAN

- **TEST SAMPLES**
  - Manufacturer: Diablo Industries, Minden NV.
  - Two representative substrate designs:
    A001 (19 via's per substrate)
    B001 (12 via's per substrate)

- **TEST SAMPLE INSPECTION**
  - Visual per MIL-STD-883, Method 2032.
  - Film adhesion test.

- **ELECTRICAL TEST CONFIGURATION**
  - 2 substrates (A001) will be assembled per drawing no. A001-AMP.
  - Amplifier A001-AMP is chosen for it's operational bandwidth.

- **ENVIRONMENTAL TEST CONFIGURATION**
  - 4 housings will be assembled as follows:
    Housing A (5) substrates, A001 with filled via's.
    Housing B (5) substrates, A001 with un-filled via's (control sample)
    Housing C (5) substrates, B001 with filled via's.
    Housing D (5) substrates, B001 with un-filled via's (control sample)
  - See Figure 1.



FILLED VIA QUALIFICATION PLAN

- **ELECTRICAL TEST**
  1. Assemble per drawing no. A001-AMP.
  2. Tune and test (ambient).
  3. Temp cycle: 20 cycles, -65 to 150C (non-operating).
  4. Temp cycle: 20 cycles, -55 to 85C (non-operating).
  5. Temp cycle: 1 cycle, -55 to 85C (operating, continuously monitored).

- **ENVIRONMENTAL TEST**
  1. Monitor 4 via's per substrate (total of 20 via's).
  2. Hi-resolution photo of each monitored via's.
  3. Temp cycle: 5 cycles, liquid nitrogen (-196C) to boiling water (100C).
     - Dwell time in LN_2: Approx. 90 sec, or when LN_2 ceases to boil.
     - Dwell time in H_2O: Approx. 90 sec, or when H_2O comes to a full boil.
     - Transfer time: Immediate.
  4. Inspect each monitored via and compare to baseline photo for changes
  5. If no change, repeat steps 3 & 4 (2) times for a total of 15 cycles.
  6. After the 15th cycle, repeat step 2 for before and after records.
  7. Electrical resistance measurements.
     - Measure and record resistance between associated pad and backside ground plane for each monitored via location.
     - See Figures 2 & 3.

FILLED VIA QUALIFICATION PLAN

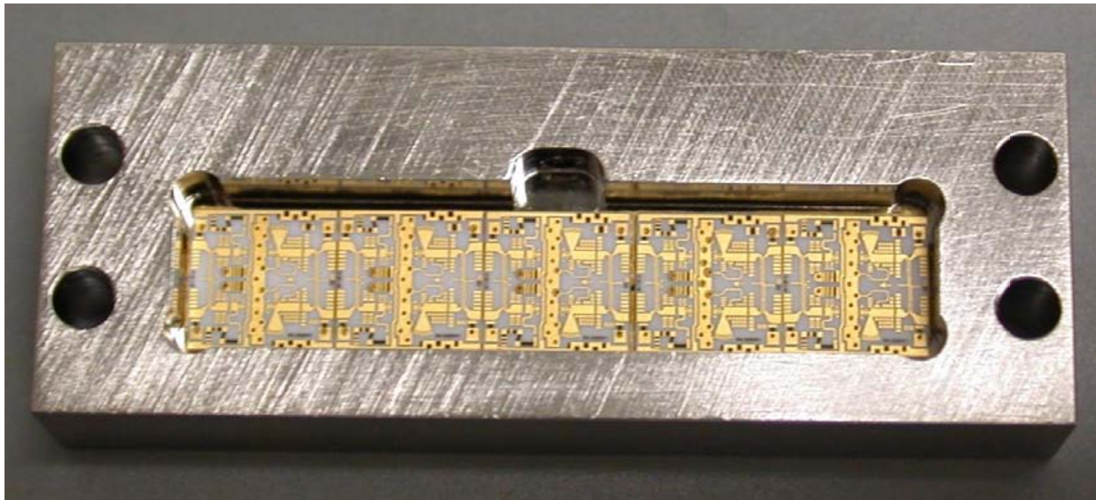


Figure 1

FILLED VIA QUALIFICATION PLAN

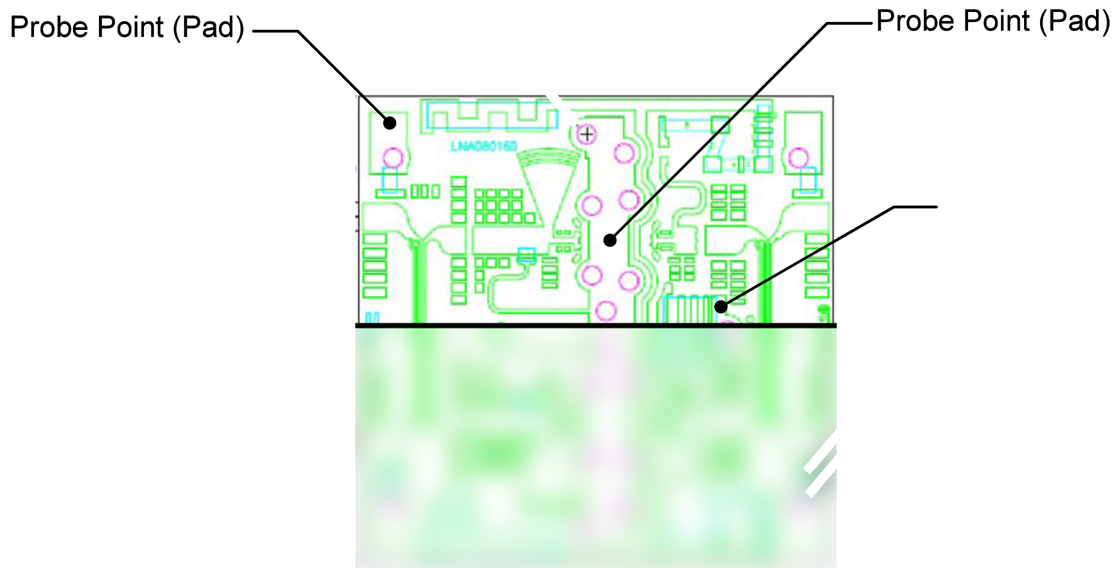


FIGURE 2
Substrate 210110

Probe Instruction: Probe resistance between pad and backside ground plane.
Do not probe via directly.

FILLED VIA QUALIFICATION PLAN

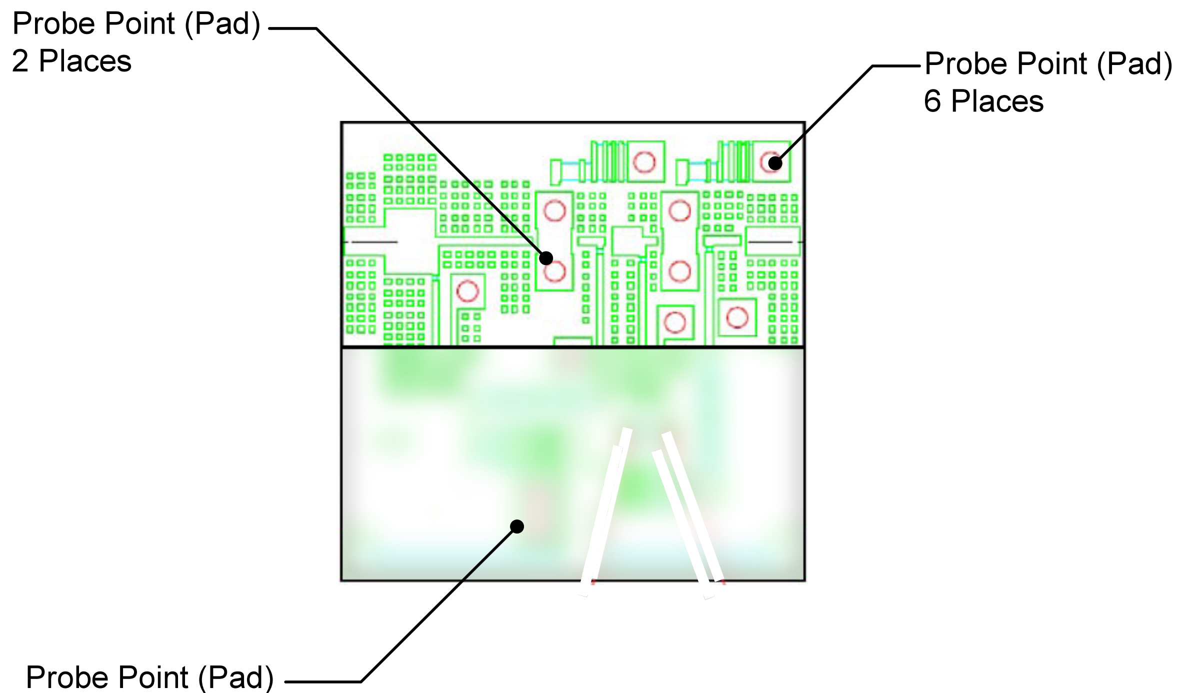
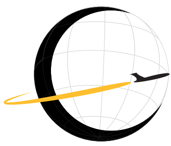


FIGURE 3
Substrate 210186

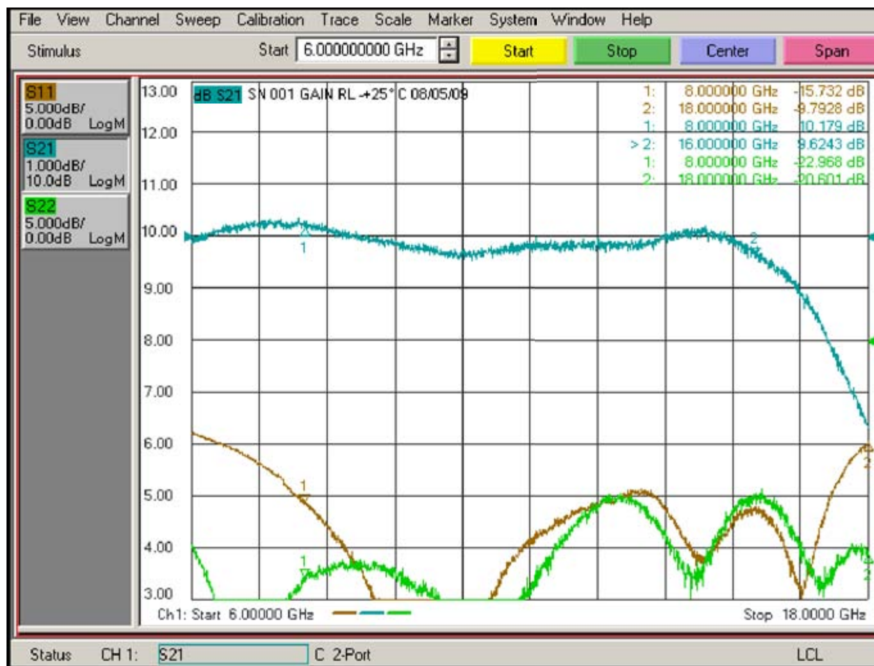
Probe Instruction: Probe resistance between pad and backside ground plane.
Do not probe via directly.

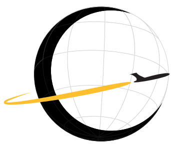
APPENDIX B

FUNCTIONAL TEST SAMPLE PERFORMANCE OVER TEMPERATURE

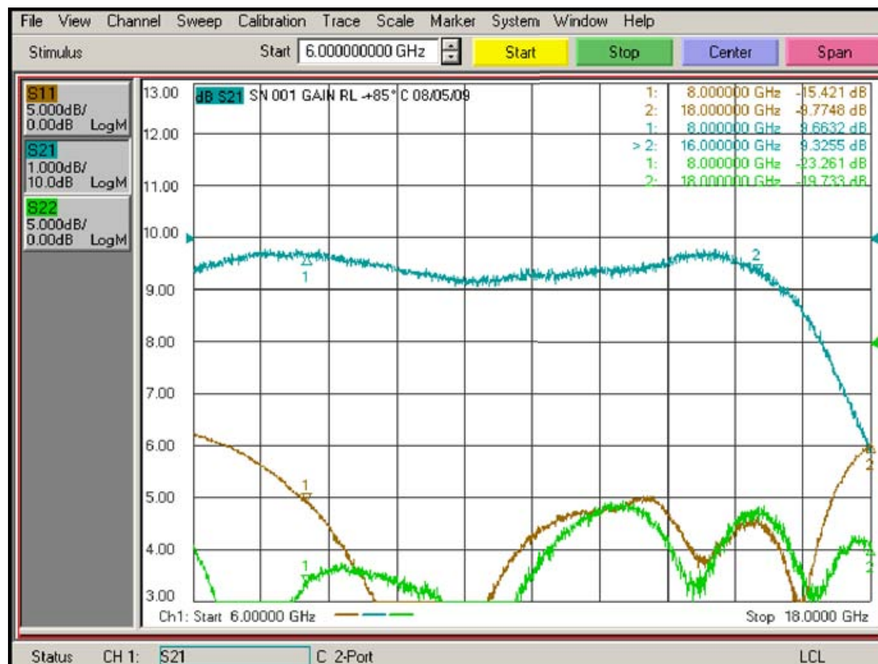


FUNCTIONAL TEST SAMPLE SN 001 (25C)

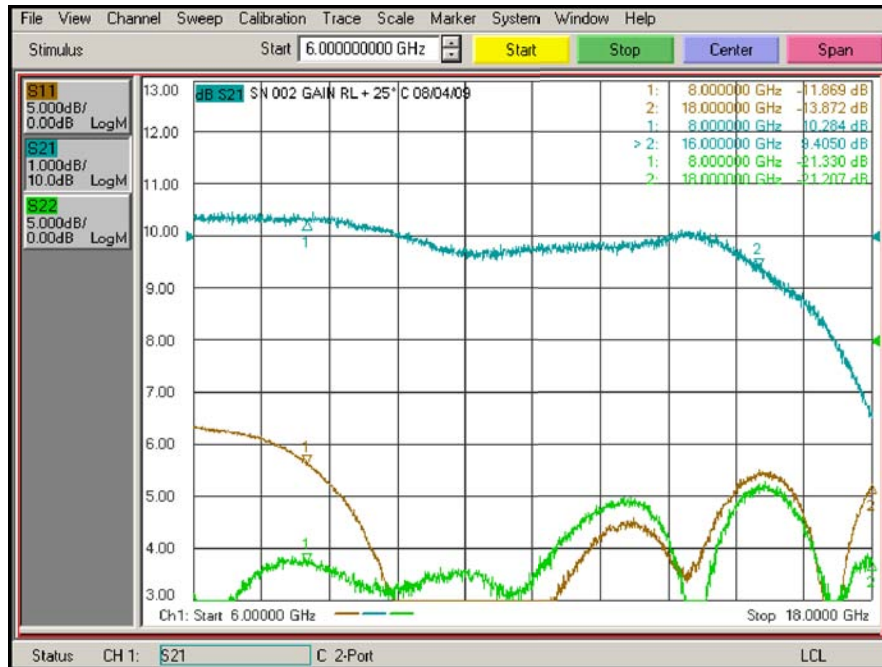


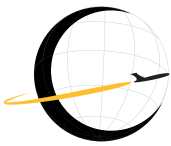


FUNCTIONAL TEST SAMPLE SN 001 (-55C & 85C)



FUNCTIONAL TEST SAMPLE SN 002 (25C)





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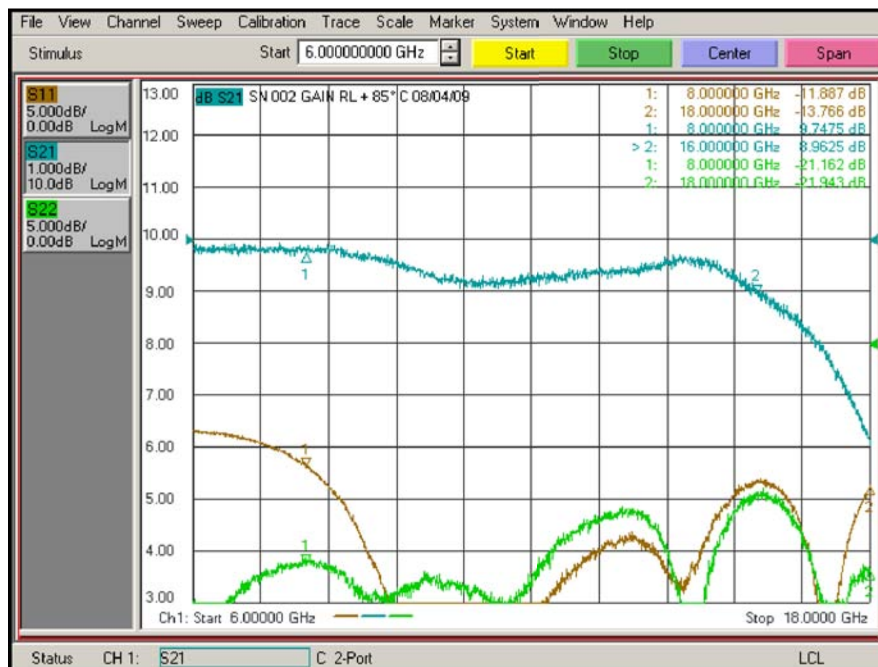
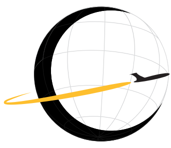
FUNCTIONAL TEST SAMPLE SN 002 (-55C & 85C)





ADDENDUM A

FILLED VIA QUALIFICATION REPORT

Die Shear Testing

ADDENDUM A
Die Shear Testing

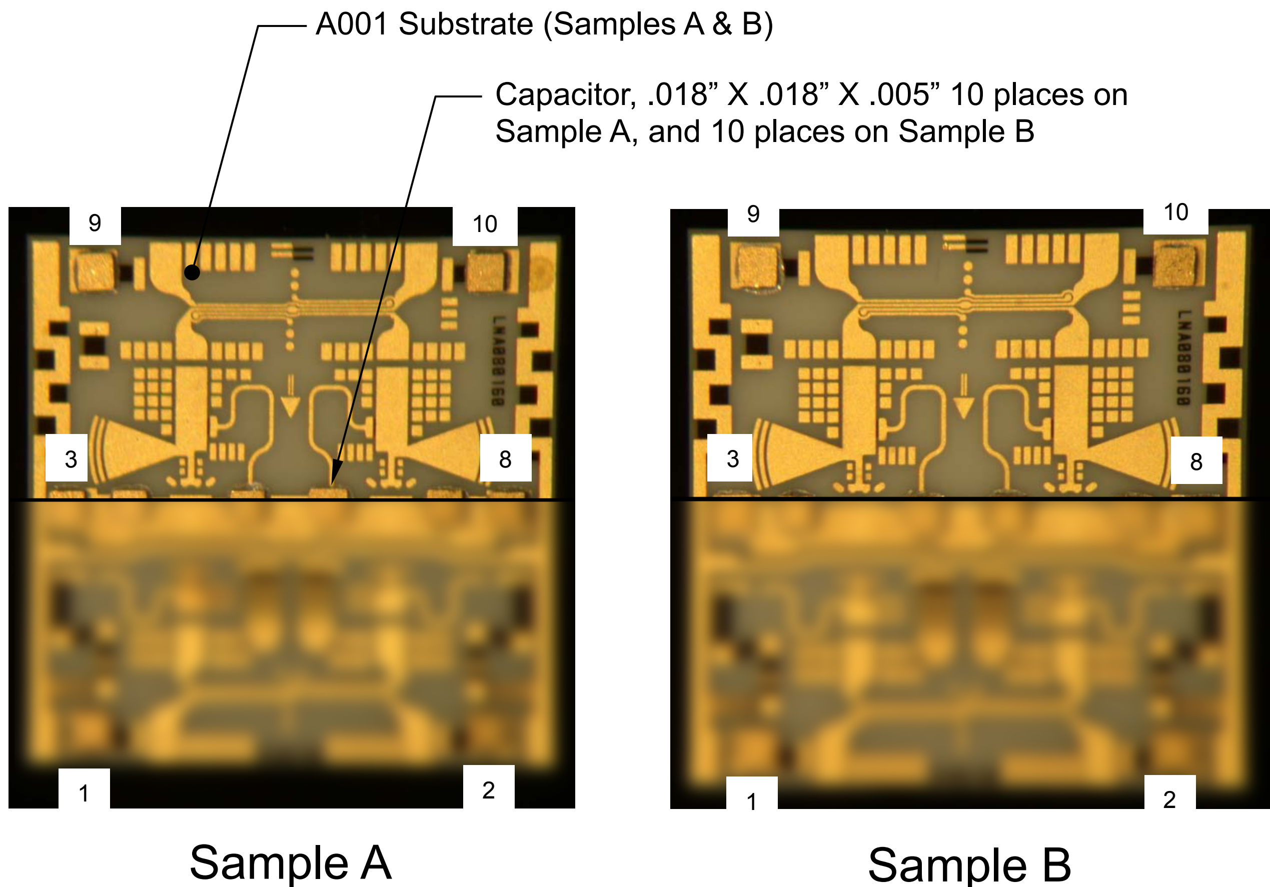
INTRODUCTION

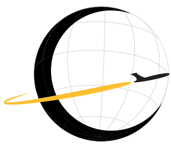
As a supplement to the Filled Via Qualification Report, die shear testing was added to evaluate the attachment of components directly over filled vias.

QUALIFICATION PLAN

Test samples: (2) A001 substrates with (10) capacitors attached to each per LPS-AB-01 using EC epoxy.

Tests:
1. Die shear (5) capacitors on Sample A, and (5) capacitors on Sample B.
2. Temperature cycle Samples A & B from -65C to 125C, 20 cycles (Table 1).
3. Die shear (5) capacitors on Sample A, and (5) capacitors on Sample B.
4. Compare die shear values to EC die shear strength for epoxy (Table 2).





Filled via substrates - Die attach
Thermal Cycle testing

Loc / Sample	Die shear (g) Before cycle	Die shear (g) After cycle
1-A		1617 (D)
1-B	958 (C)	
2-A	597 (B)	
2-B		990 (D)
3-A	824 (D)	
3-B		855 (D)
4-A	758(C)	
4-B		1130 (B)
5-A		974 (C)
5-B	807 (D)	
6-A	978 (D)	
6-B	1268 (D)	
7-A		1039 (B)
7-B	952 (D)	
8-A		1224 (D)
8-B	1098 (D)	
9-A		1040 (C)
9-B	998 (D)	
10-A	918 (C)	
10-B		831 (B)
Average	**923**	**1070**
Shear force	6278psi	7327psi

Note: 6 (vs. 5) capacitors were inadvertently die sheared from Sample B for the pre sample test.

Test Parameter	Setting
Hot	+125C (dwell 10 minutes Min)
Cold	-65C (dwell 10 minutes Min)
Cycles	20

Failure Mode Code	Description
B	Die broke
C	Epoxy separated from part
D	Epoxy separated from substrate

Requirements:
- Die shear strength EC: 3450psi min.
- MIL-STD-883 Method 2019.7: 800psi min.

Results:
- All parts exceed die shear requirements.
- No change after temperature cycling.

Conclusion:
- Component attachment over filled vias, as qualified herein, is qualified for use in space borne microelectronic circuits.