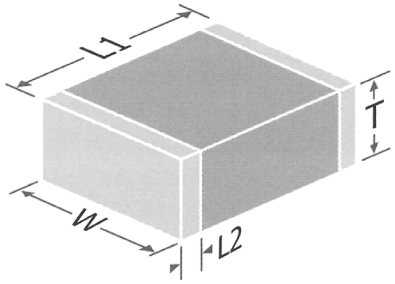
FM2

FM2 Range of Non-Magnetic Low ESR X7R Capacitors

FM2 Non-magnetic Range

A range of X7R MLC capacitors with a guaranteed non-magnetic / relative permeability of 1.000 and having a customised design to achieve a lower ESR and improved Q factor than normal X7R MLCC's. Ideal for critical applications such as NMR / MRI and where PIM could potentially be an issue if nickel was present. These MLCC's can be used where an improved performance is required, such as blocking caps.

Electrical Details	
	FM2
Capacitance Range	100pF – 120nF
Temperature Coefficient of Capacitance (TCC)	±15% from -55°C to +125°C
Insulation Resistance (IR)	100GΩ or 1000secs (whichever is the less)
Dielectric Withstand Voltage (DWV)	Voltage applied for 5 ±1 seconds, 50mA charging current maximum
Operating temperature range	-55ºC / +125ºC
Ageing Rate	<2% per decade



Range Dimensions – FM2 Non-magnetic Range

Size	Length (L1) mm/inches	Width (W) mm/inches	Max. Thickness (T) mm/inches	Termination Band (L2) mm/inches	
				min	max
0402	1.0 ± 0.10 0.04 ± 0.006	0.50 ± 0.10 0.02 ± 0.003	0.60 0.031	0.10 0.004	0.40 0.015
0505	1.4 +0.35 -0.25 0.055 +0.014 -0.010	1.4 ± 0.25 0.055 ± 0.010	1.27 0.050	0.13 0.005	0.5 0.020
0603	1.6 ± 0.2 0.063 ± 0.008	0.8 ± 0.2 0.031 ± 0.008	0.7 0.028	0.10 0.004	0.40 0.015
0805	2.0 ± 0.3 0.08 ± 0.012	1.25 ± 0.2 0.05 ± 0.008	1.0 0.039	0.13 0.005	0.75 0.03

Knowles Precision Devices Sales contact e-mail	Europe:	KPD-Europe-sales@knowles.com
	Asia:	KPD-Asia-sales@knowles.com
	USA:	KPD-NA-sales@knowles.com

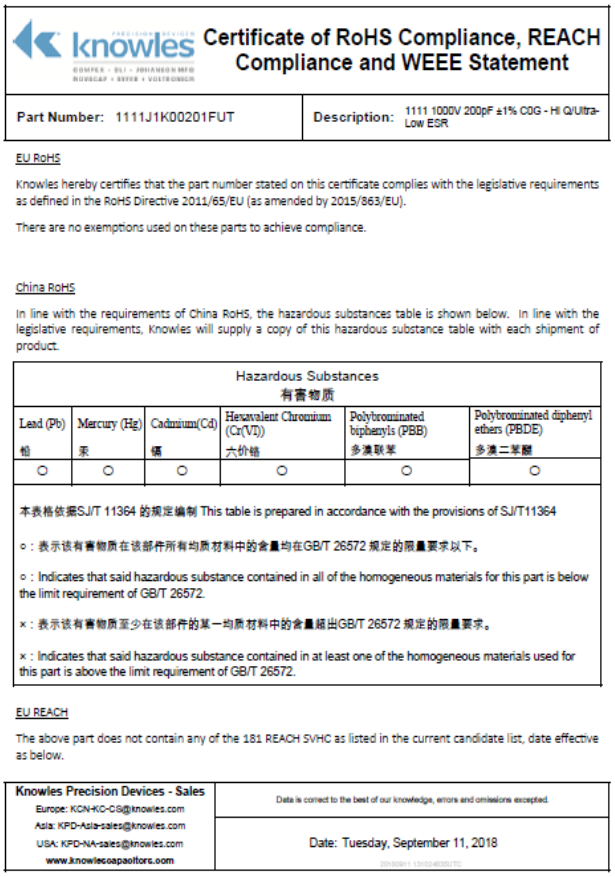
Ordering Information – FM2 Non-magnetic Range

0603	2	100	0183	K	X	T	FM2
Chip Size	**Termination**	**Voltage d.c. (marking code)**	**Capacitance in Pico farads (pF)**	**Capacitance Tolerance**	**Dielectric Codes**	**Packaging**	**Suffix**
0402 **0505** **0603** **0805**	**2** = Sintered silver base with copper barrier (100% matte tin plating). RoHS compliant. Available on High Q only.	**050** = 50V **063** = 63V **100** = 100V **200** = 200V **250** = 250V **500** = 500V **1K0** = 1kV	<1.0pF Insert a P for the decimal point as the first character. e.g., **P300** = 0.3pF Values in 0.1pF steps ≥1.0pF & <10pF Insert a P for the decimal point as the second character. e.g., **8P20** = 8.2pF Values are E24 series ≥10pF First digit is 0. Second and third digits are significant figures of capacitance code. The fourth digit is the number of zeros following. e.g., **0101** = 100 pF Values are E24 series	**J**: ± 5% **K**: ± 10% **M** ± 20%	**X** = X7R	**T** = 178mm (7") reel **R** = 330mm (13") reel **B** = Bulk pack – tubs or trays	**FM2** = Low Loss improved performance

Minimum/Maximum Capacitance Values – FM2 Non-magnetic Range

Chip Size	0402	0505	0603	0805
Min Cap	100pF	100pF	100pF	330pF
50	10nF	150nF	47nF	120nF
63V	10nF	120nF	47nF	68nF
100V	6.8nF	68nF	18nF	68nF
200V	1.8nF	47nF	15nF	47nF
250V	1.8nF	47nF	15nF	47nF
500V	-	15nF	3.3nF	15nF
1000V	-	-	-	8.2nF
Tape quantities	7" Reel 10000	7" Reel 2500	7" Reel 4000	7" Reel 3000

Detailed individual datasheets and part specific environmental certificates can be downloaded direct from the KPD website – www.knowlescapacitors.com



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Certificate of RoHS Compliance, REACH Compliance and WEEE Statement

Part Number: 1111J1K00201FUT	Description: 1111 1000V 200pF ±1% C0G - HI Q/Ultra-Low ESR

EU RoHS

Knowles hereby certifies that the part number stated on this certificate complies with the legislative requirements as defined in the RoHS Directive 2011/65/EU (as amended by 2015/863/EU).

There are no exemptions used on these parts to achieve compliance.

China RoHS

In line with the requirements of China RoHS, the hazardous substances table is shown below. In line with the legislative requirements, Knowles will supply a copy of this hazardous substance table with each shipment of product.

Hazardous Substances 有害物质

Lead (Pb) 铅	Mercury (Hg) 汞	Cadmium(Cd) 镉	Hexavalent Chromium (Cr(VI)) 六价铬	Polybrominated biphenyls (PBB) 多溴联苯	Polybrominated diphenyl ethers (PBDE) 多溴二苯醚
O	O	O	O	O	O

本表格依据SJ/T 11364 的规定编制 This table is prepared in accordance with the provisions of SJ/T11364

o：表示该有害物质在该部件所有均质材料中的含量均在GB/T 26572 规定的限量要求以下。

o : Indicates that said hazardous substance contained in all of the homogeneous materials for this part is below the limit requirement of GB/T 26572.

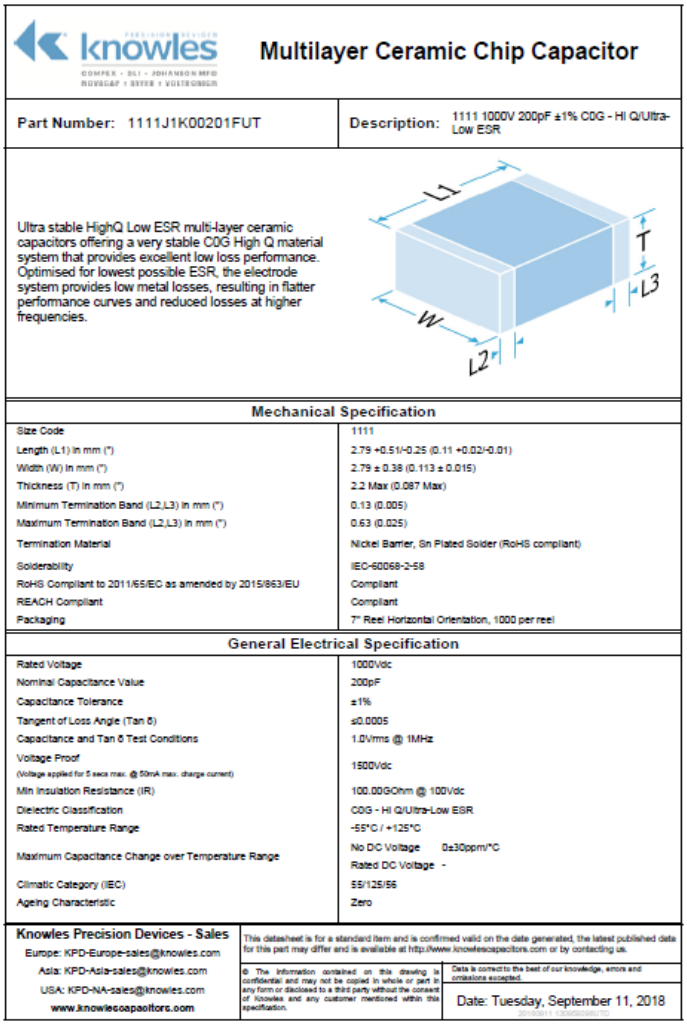
×：表示该有害物质至少在该部件的某一均质材料中的含量超出GB/T 26572 规定的限量要求。

× : Indicates that said hazardous substance contained in at least one of the homogeneous materials used for this part is above the limit requirement of GB/T 26572.

EU REACH

The above part does not contain any of the 181 REACH SVHC as listed in the current candidate list, date effective as below.

Knowles Precision Devices - Sales Europe: KCN-KC-CG@knowles.com Asia: KPD-Asia-sales@knowles.com USA: KPD-NA-sales@knowles.com www.knowlescapacitors.com	Data is correct to the best of our knowledge, errors and omissions excepted. Date: Tuesday, September 11, 2018



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Multilayer Ceramic Chip Capacitor

Part Number: 1111J1K00201FUT	Description: 1111 1000V 200pF ±1% C0G - HI Q/Ultra-Low ESR

Ultra stable HighQ Low ESR multi-layer ceramic capacitors offering a very stable C0G High Q material system that provides excellent low loss performance. Optimised for lowest possible ESR, the electrode system provides low metal losses, resulting in flatter performance curves and reduced losses at higher frequencies.

Mechanical Specification

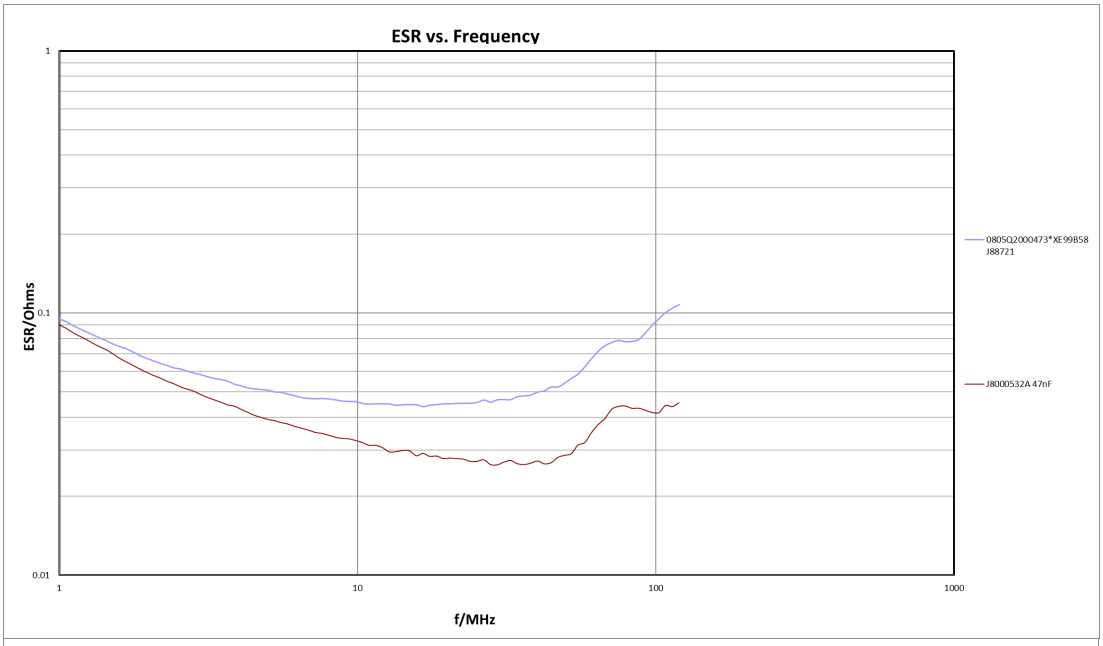
Size Code	1111
Length (L1) in mm (")	2.79 +0.51/-0.25 (0.11 +0.02/-0.01)
Width (W) in mm (")	2.79 ± 0.38 (0.113 ± 0.015)
Thickness (T) in mm (")	2.2 Max (0.087 Max)
Minimum Termination Band (L2,L3) in mm (")	0.13 (0.005)
Maximum Termination Band (L2,L3) in mm (")	0.63 (0.025)
Termination Material	Nickel Barrier, Sn Plated Solder (RoHS compliant)
Solderability	IEC-60068-2-58
RoHS Compliant to 2011/65/EC as amended by 2015/863/EU	Compliant
REACH Compliant	Compliant
Packaging	7" Reel Horizontal Orientation, 1000 per reel

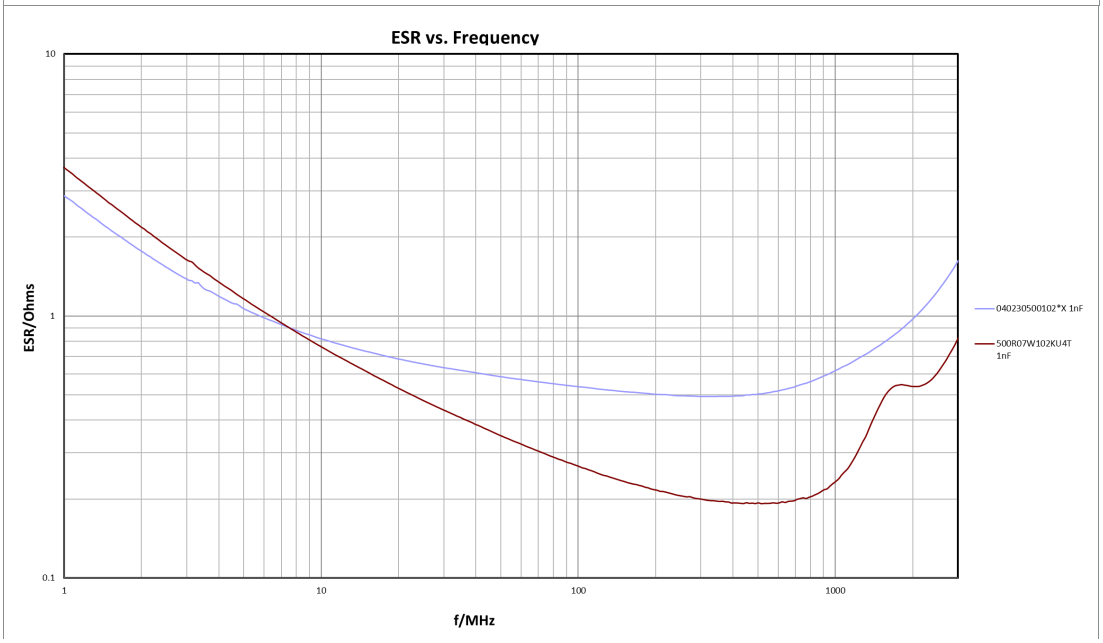
General Electrical Specification

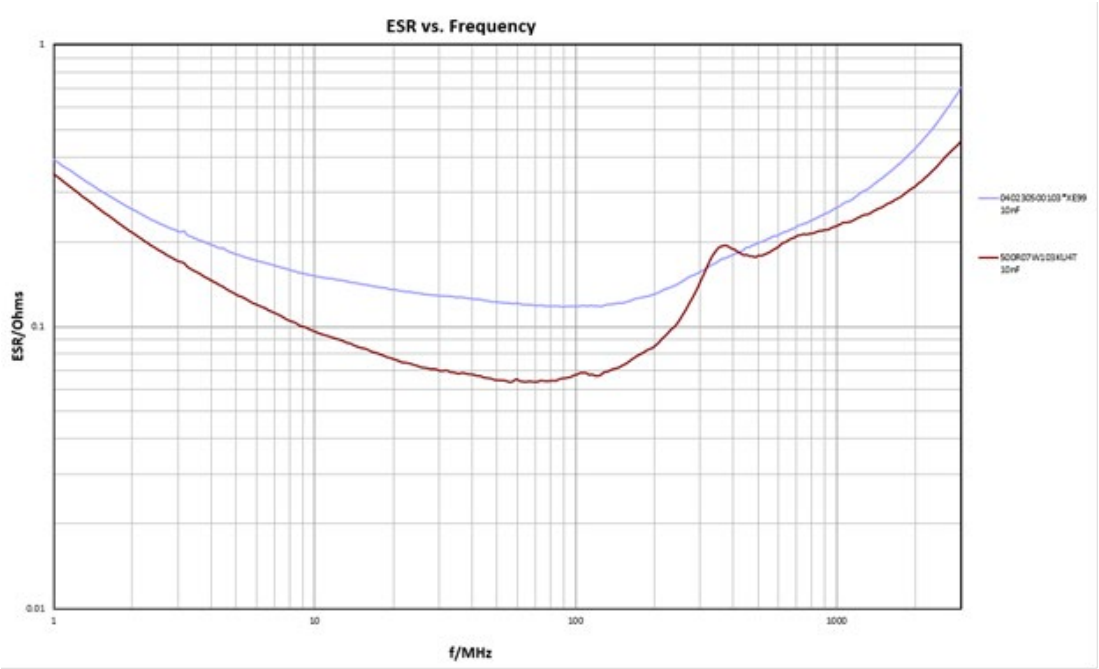
Rated Voltage	1000Vdc
Nominal Capacitance Value	200pF
Capacitance Tolerance	±1%
Tangent of Loss Angle (Tan δ)	≤0.0005
Capacitance and Tan δ Test Conditions	1.0Vrms @ 1MHz
Voltage Proof (Voltage applied for 5 secs max. @ 50mA max. charge current)	1500Vdc
Min Insulation Resistance (IR)	100.00GOhm @ 100Vdc
Dielectric Classification	C0G - HI Q/Ultra-Low ESR
Rated Temperature Range	-55°C / +125°C
Maximum Capacitance Change over Temperature Range	No DC Voltage 0±30ppm/°C Rated DC Voltage -
Climatic Category (IEC)	55/125/56
Ageing Characteristic	Zero

Knowles Precision Devices - Sales Europe: KPD-Europe-sales@knowles.com Asia: KPD-Asia-sales@knowles.com USA: KPD-NA-sales@knowles.com www.knowlescapacitors.com	This datasheet is for a standard item and is confirmed valid on the date generated, the latest published data for this part may differ and is available at http://www.knowlescapacitors.com or by contacting us. © The information contained on this drawing is confidential and may not be copied in whole or part in any form or disclosed to a third party without the consent of Knowles and any customer mentioned within this specification. Data is correct to the best of our knowledge, errors and omissions excepted. Date: Tuesday, September 11, 2018

Typical Performance Curves – "FM2" range of X7R low ESR Capacitors







Note curves are typical, based on data measured using a Keysight E4991 impedance analyser and Keysight 16197A test fixture Actual performance in circuit may differ and parts should be tested in application.

Performance and Testing

	Hi Q			C0G/NP0			X7R		
	Ultra-stable			Ultra-stable			Stable		
IECQ-CECC	1B/CG	-	-	1B/CG	-	-	2C1	2R1	2X1
EIA	-	C0G/NP0	-	-	C0G/NP0	-	-	X7R	-
MIL	-	-	CG (BP)	-	-	CG (BP)	BZ	-	BX
Rated temperature range	-55ºC to +125ºC / -55ºC to +175ºC (H17)			-55ºC to +125ºC			-55ºC to +125ºC		
Maximum capacitance change over temperature range	0 ± 30 ppm/ºC			0 ± 30 ppm/ºC			± 20%	± 15%	± 15%
Rated DC voltage applied							+20 -30%	-	+15 -25%
Knowles / Syfer dielectric ordering code	Q			C			R	X	B
Tangent of loss angle (tan δ)	≤ 0.0005 @ 1MHz (Cr ≤ 1nF) or 1kHz (Cr > 1nF)			Cr > 50pF ≤ 0.0015 Cr ≤ 50pF = 0.0015 (15 + 0.7) Cr @ 1MHz (Cr ≤ 1nF) or 1kHz (Cr > 1nF)			≤ 0.025 @ 1kHz		
Insulation resistance (Ri) OR Time constant (Ri*Cr) (whichever is the least)	100GΩ or 1000s			100GΩ or 1000s			100GΩ or 1000s		
Capacitance tolerance (ordering code)	Cr <4.7pF	± 0.05pF (H) ± 0.10pF (B) ± 0.25pF (C) ± 0.50pF (D)		Cr <4.7pF	± 0.05pF (H) ± 0.10pF (B) ± 0.25pF (C) ± 0.50pF (D)		± 5% (J) ± 10% (K) ± 20% (M)		
	Cr <10pF	± 0.10pF (B) ± 0.25pF (C) ± 0.50pF (D)		Cr <10pF	± 0.10pF (B) ± 0.25pF (C) ± 0.50pF (D)				
	Cr ≥10pF	± 1% (F) ± 2% (G) ± 5% (J) ± 10% (K)		Cr ≥10pF	± 1% (F) ± 2% (G) ± 5% (J) ± 10% (K)				
Dielectric strength	Voltage applied for 5 seconds max. Charging current limited to 50mA maximum.								
<200V **>200V to <500V** **500V to <1000V** **500V to <1000V** **>1kV to <1200V** **>1200V** **>1000V**	2.5 times Rated voltage + 250V 1.5 times - 1.25 times 1.2 times -			2.5 times Rated voltage + 250V 1.5 times - 1.25 times 1.2 times -			2.5 times Rated voltage + 250V - 1.5 times - - 1.2 times		
Climatic category (IEC)									
Chip	55/125/56 55/175/56 (H17)			55/125/56			55/125/56		
Ageing characteristic (Typical)	Zero			Zero			<2% per time decade		

Soldering Information

Knowles (Syfer) MLCCs are compatible with all recognised soldering/mounting methods for chip capacitors. A detailed application note is available at www.knowlescapacitors.com

Reflow Soldering

Knowles recommend reflow soldering as the preferred method for mounting MLCCs. Knowles (Syfer) MLCCs can be reflow soldered using the internationally recognised reflow profile defined in IPC/FEDEC J-STD-020. Sn plated termination chip capacitors are compatible with both conventional and lead free soldering with peak temperatures of 260ºC to 270ºC acceptable.

The heating ramp rate should be such that components see a temperature rise of 1.5ºC to 4ºC per second to maintain temperature uniformity through the MLCC.

The time for which the solder is molten should be maintained at a minimum, so as to prevent solder leaching. Extended times above 230˚C can cause problems with oxidation of Sn plating. Use of an inert atmosphere can help if this problem is encountered. Palladium/Silver (Pd/Ag) terminations can be particularly susceptible to leaching with free lead, tin rich solders and trials are recommended for this combination.

Cooling to ambient temperature should be allowed to occur naturally, particularly if larger chip sizes are being soldered. Natural cooling allows a gradual relaxation of thermal mismatch stresses in the solder joints. Forced cooling should be avoided as this can induce thermal breakage.

IPC / J-STD-020D Reflow Specification

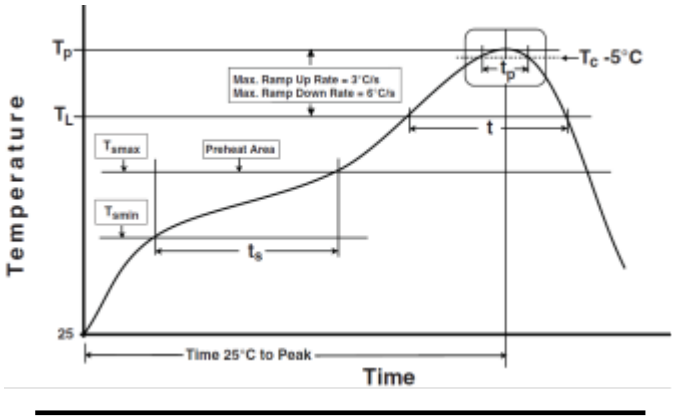
SnPb Classification Temperature		
Package Thickness	Volume mm³ <350	Volume mm³ ≥350
<2.5mm	235˚C	220˚C
≥2.5mm	220˚C	220˚C

Pb Free Classification Temperature			
Package Thickness	Volume mm³ <350	Volume mm³ 350 – 2000	Volume mm³ >2000
<1.6mm	260˚C	260˚C	260˚C
1.6mm – 2.5mm	260˚C	250˚C	245˚C
>2.5mm	250˚C	245˚C	245˚C

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100˚C 150˚C 60 – 120 seconds	150˚C 200˚C 60 – 120 seconds
Average ramp-up rate (T_{smax} to T_p)	3˚C/second max	3˚C/second max
Liquidous temperature (T_L) Time at liquidous (t_L)	183˚C 60 – 150 seconds	217˚C 60 – 150 seconds
Peak package body temperature (T_p)	See classification in temp Table above	See classification in temp Table above
Time (t_p) within 5˚C of the specified classification temperature (T_c)	20 seconds	30 seconds
Average ramp-down rate (T_p to T_{smax})	6˚C/second max.	6˚C/second max.
Time 25˚C to peak temperature	6 minutes max.	8 minutes max.

Reflow profiles in this document are for recommended limits. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in the Table above

We cannot give a definitive profile of the actual peak temperatures, as this is dependent on a number of factors which can only be decided by the assembler – the type of solder used, the size, specification and arrangement of other components on the board and the overall thermal mass of the board.



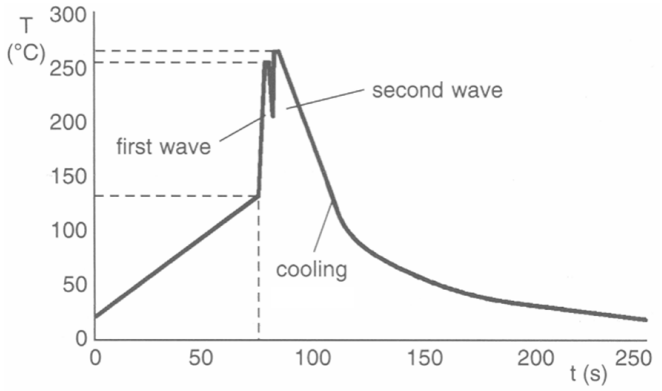
Wave Soldering

Wave soldering is generally acceptable, but the thermal stresses caused by the wave have been shown to lead to potential problems with larger or thicker chips. Particular care should be taken when soldering SM chips larger than size 1210 and with a thickness greater than 1.0mm for this reason.

Maximum permissible wave temperature is 270˚C for SM chips.

The total immersion time in solder should be kept to a minimum. It is strongly recommended that Sn/Ni plated terminations are specified for wave soldering applications

If wave soldering is to be carried out, we recommend a profile of the general shape as below (single wave of the same general shape is also acceptable).



Total immersion exposure time for Sn/Ni terminations is 30s at a wave temperature of 260ºC. Note that for multiple soldering operations, including the rework, the soldering time is cumulative.

Rework of Chip Capacitors

Syfer recommend hot air/gas as the preferred method of applying heat for rework. Apply even heat surrounding the component to minimise internal thermal gradients. Soldering irons or other techniques that apply direct heat to the chip or surrounding area should not be used as these can result in micro cracks being generated.

Minimise the rework heat duration and allow components to cool naturally after soldering.

Use of Silver Loaded Epoxy Adhesives

Chip capacitors can be mounted to circuit boards using silver loaded adhesive provided the termination material of the capacitor is selected to be compatible with the adhesive. This is normally PdAg. Standard tin finishes are often not recommended for use with silver loaded epoxies as there can be electrical and mechanical issues with the joint integrity due to material mismatch.

Handling & Storage

Components should never be handled with fingers; perspiration and skin oils can inhibit solderability and will aggravate cleaning.

Chip capacitors should never be handled with metallic instruments. Metal tweezers should never be used as these can chip the product and leave abraded metal tracks on the product surface. Plastic or plastic coated metal types are readily available and recommended – these should be used with an absolute minimum of applied pressure.

Incorrect storage can lead to problems for the user. Rapid tarnishing of the terminations, with an associated degradation of solderability, will occur if the product comes into contact with industrial gases such as sulphur dioxide and chlorine. Storage in free air, particularly moist or polluted air, can result in termination oxidation.

Packaging should not be opened until the MLCs are required for use. If opened, the pack should be re-sealed as soon as practicable. Alternatively, the contents could be kept in a sealed container with an environmental control agent.

Long term storage conditions, ideally, should be temperature controlled between -5 and +40°C and humidity controlled between 40% and 60% R.H.

Taped product should be stored out of direct sunlight, which might promote deterioration in tape or adhesive performance.

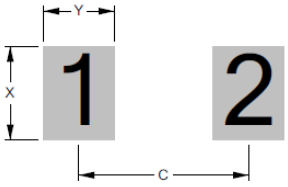
Product, stored under the conditions recommended above, in its "as received" packaging, has a minimum shelf life of 2 years.

SM Pad Design

Knowles (Syfer) conventional 2-terminal chip capacitors can generally be mounted using pad designs in accordance with international specification IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standards, but there are some other factors that have been shown to reduce mechanical stress, such as reducing the pad width to less than the chip width. In addition, the position of the chip on the board should also be considered.

IPC-7351 pad design for 0603, 0805 & 1111 MLCC

	0603	0805	1111
C	1.60	1.80	2.80
Y	0.85	1.15	1.20
X	1.00	1.45	3.20



Mechanical Cracking considerations

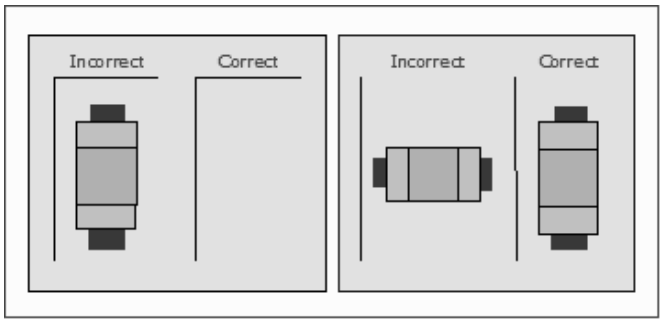
Mechanical cracking is one of the main causes of failure in MLCC's. Some design considerations can reduce the instances of mechanical cracking.

Assembly Design/ Manufacture Considerations

Mechanical stress can be influenced by a number of different factors associated with the design of the assembly and assembly manufacture. These factors include:

- PCB design – copper power and ground planes.
- A PCB design resulting in an uneven metal distribution (usually caused by large power or ground planes) can result in PCB warpage during the soldering process caused by the different Thermal Coefficient of Expansion rates between the copper and the epoxy fibre glass. If large power/ ground planes are required then cross hatching the copper area may prove to be useful.
- Position/ orientation of the capacitor on the PCB in relation to the edge of the PCB and other components/ attachments.

PCB Corner PCB Edge

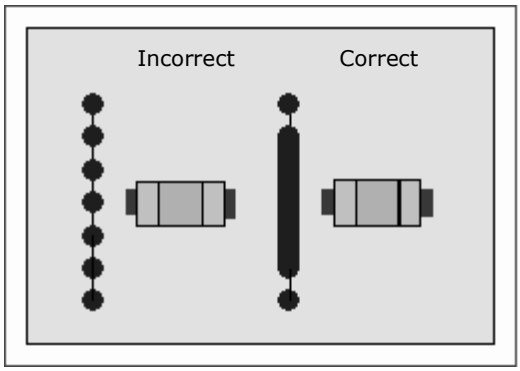


Capacitor placement not recommended in the corner of the PCB.

Recommended capacitor orientation with respect to PCB edge (denoted by black lines).

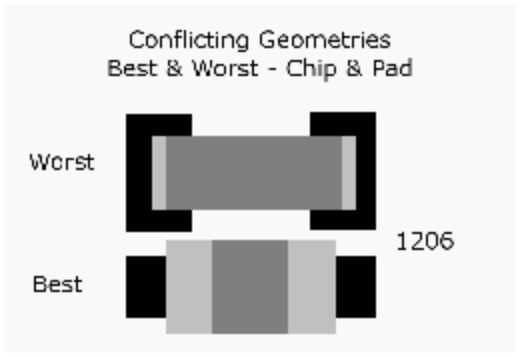
Note: Stress zone is typically within 5mm of PCB edge or fixing point.

Use of PCB Slots



Using a slot along the depanelisation edge reduces the level of stress exerted onto the capacitor by approximately 50%.

Solder pad/ land sizes



Reducing the pad/ land size can reduce the level of stress exerted onto the capacitor by approximately 50%.

Use of adhesives

Depending upon the type of adhesive used, the effect can be a significant reduction in the bend strength of a capacitor. For example, during experiments approximately 50% of the PCB bend was required to crack a capacitor fixed with adhesive when compared to a capacitor not fixed with adhesive.

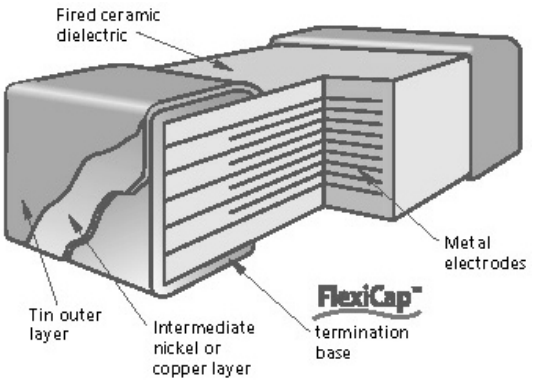
FlexiCap™ Termination

FlexiCap™ has been developed as a result of listening to customer's experiences of stress damage to MLCCs from many manufacturers, often caused by variations in production processes.

Our answer is a proprietary flexible epoxy polymer termination material that is applied to the device under the usual nickel barrier finish. FlexiCap™ will accommodate a greater degree of board bending than conventional capacitors.

Ranges are available with FlexiCap™ termination material offering increased reliability and superior mechanical performance (board flex and temperature cycling) when compared with standard termination materials. Refer to Syfer application note reference AN0001. FlexiCap™ capacitors enable the board to be bent almost twice as much as before mechanical cracking occurs. Refer to application note AN0002.

FlexiCap™ is also suitable for space applications having passed thermal vacuum outgassing tests. Refer to Syfer application note reference AN0026.



FlexiCap™ MLCC cross section

Syfer has delivered millions of FlexiCap™ components and during that time has collected substantial test and reliability data, working in partnership with customers world wide, to eliminate mechanical cracking.

An additional benefit of FlexiCap™ is that MLCCs can withstand temperature cycling from -55 to 125°C in excess of 1,000 times without cracking.

FlexiCap™ termination has no adverse effect on any electrical parameters, nor affects the operation of the MLCC in any way.

Application Notes

FlexiCap™ may be handled, stored and transported in the same manner as standard terminated capacitors. The requirements for mounting and soldering FlexiCap™ are the same as for standard SMD capacitors.

For customers currently using standard terminated capacitors there should be requirement to change the assembly process when converting to FlexiCap™.

Based upon the board bend tests in accordance with IEC 60384-1 the amount of board bending required to mechanically crack a FlexiCap™ terminated capacitor is significantly increased compared with standard terminated capacitors.

Product: X7R	Typical bend performance under AEC-Q200 test conditions
Standard Termination	2mm to 3mm
FlexiCap™	Typically 8mm to 10mm

REACH (Registration, Evaluation, Authorisation and restriction of Chemicals) Statement

The main purpose of REACH is to improve the protection of human health and the environment from the risks arising from the use of chemicals.

Syfer Technology Ltd maintains both ISO 14001, Environmental Management System and OHSAS 18001 Health & Safety Management System approvals that require and ensure compliance with corresponding legislation such as REACH.

For further information, please contact the sales office at SyferSales@knowles.com

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RoHS Compliance

Syfer routinely monitors world wide material restrictions (e.g., EU/China and Korea RoHS mandates) and is actively involved in shaping future legislation.

All standard C0G/NPO, X7R, X5R and High Q Syfer MLCC products are compliant with the EU RoHS directive (see below for special exemptions) and those with plated terminations are suitable for soldering common lead free solder alloys (refer to 'Soldering Information' for more details on soldering limitations). Compliance with EU RoHS directive automatically signifies compliance with some other legislation (e.g., Korea RoHS). Please refer to the Sales Office for details of compliance with other materials legislation.

Breakdown of material content, SGS analysis reports and tin whisker test results are available on request.

Most Syfer MLCC components are available with non-RoHS compliant tin/lead (SnPb) Solderable termination finish for exempt applications and where pure tin is not acceptable. Other tin free termination finishes may also be available – please refer to the Sales Office for further details.

X8R ranges <250Vdc are not RoHS 2011/65/EU compliant.

115Vac 400Hz ranges are not RoHS 2011/65/EU compliant.

Check the website, www.knowlescapacitors.com/syfer for latest RoHS update.

Export Controls and Dual-use Regulations

Certain Syfer catalogue components are defined as 'dual-use' items under international export controls – those that can be used for civil and military purposes which meet certain specified technical standards.

The defining criteria for a dual-use component with respect to Syfer products is one with a voltage rating of >750V and a capacitance value >250nF and a series inductance <10nH.

Components defined as 'dual-use' under the above criteria automatically require a licence for export outside the EU, and may require a licence for export with the EU.

The application for a licence is routine, but customers for these products will be asked to supply further information.

Please refer to the sales office if you require any further information on export restrictions.

Other special components may additionally need to comply with export regulations.

Ageing of Ceramic Capacitors

Capacitor ageing is a term used to describe the negative, logarithmic capacitance change which takes place in ceramic capacitors with time. The crystalline structure for barium titanate based ceramics changes on passing through its Curie temperature (known as the Curie Point) at about 125ºC. The domain structure relaxes with time and in doing so, the dielectric constant reduces logarithmically; this is known as the ageing mechanism of the dielectric constant. The more stable dielectrics have the lowest ageing rates.

The ageing process is reversible and repeatable. Whenever the capacitor is heated to a temperature above the Curie Point the ageing process starts again from zero.

The ageing constant, or ageing rate, is defined as the percentage loss of capacitance due to the ageing process of the dielectric which occurs during a decade of time (a tenfold increase in age) and is expressed as percent per logarithmic decade of hours. As the law of decrease of capacitance is logarithmic, this means that for a capacitor with an ageing rate of 1% per decade of time, the capacitance will decrease at a rate of:

a) 1% between 1 and 10 hours

b) An additional 1% between the following 10 and 100 hours

c) An additional 1% between the following 100 and 1000 hours

d) An additional 1% between the following 1000 and 10000 hours

e) The ageing rate continues in this manner throughout the capacitor's life.

Typical values of the ageing constant for our MLCCs are

Dielectric Class	Typical Values
Ultra Stable C0G/NP0	Negligible capacitance loss through ageing
Stable X7R	<2% per decade of time

Capacitance Measurements

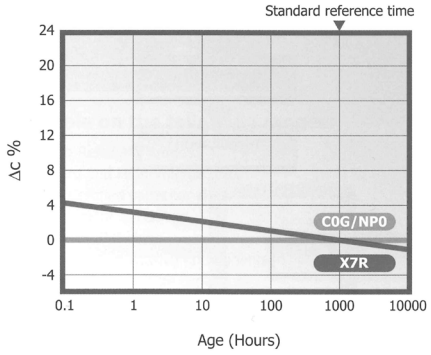
Because of ageing it is necessary to specify an age for reference measurements at which the capacitance shall be within the prescribed tolerance. This is fixed at 1000 hours, since for all practical purposes there is not much further loss of capacitance after this time.

All capacitors shipped are within their specified tolerance at the standard reference age of 1000 hours after having cooled through their Curie temperature.

The ageing curve for any ceramic dielectric is a straight line when plotted on semi-log paper.

Capacitance vs. Time

(Ageing X7R @ 1% per decade)



Tight Tolerance

One of the advantages of Syfer's unique 'wet process' of manufacture is the ability to offer capacitors with exceptionally tight capacitance tolerances.

The accuracy of the printing screens used in the fully automated, computer controlled manufacturing process allows for tolerance as close as ± 1% on C0G/NP0 parts greater than or equal to 10pF. For capacitance value less than 4.7pF tolerances can be as tight as ± 0.05pF.

Periodic Tests Conducted and Reliability Data

For standard surface mount capacitors components are randomly selected on a sample basis and the following routine tests conducted:

- Load Test. 1,000 hours @ 125°C (150°C for X8R). Applied voltage depends on components tested
- Humidity Test. 168 hours @ 85°C/85%RH
- Board Deflection (bend test)

Test results are available on request.

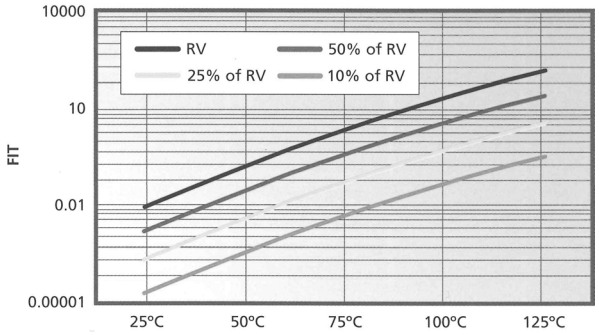
Conversion Factors

From	To	Operation
FITs	MTBF (hours)	10^9 ÷ FITs
FITs	MTBF (years)	10^9 ÷ (FITs × 8760)

FIT = Failures In Time. 1 FIT = 1 failure in 10^9 hours

MTBF = Mean Time Between Failure

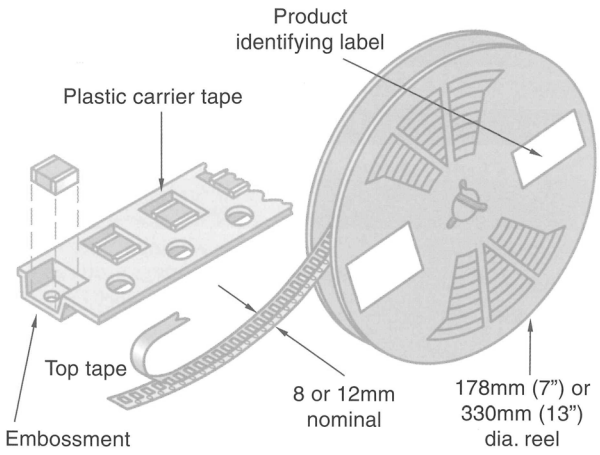
Example of FIT Data Available



Component type:	0805 (C0G/NP0 and X7R)
Testing Location:	Syfer reliability test department
Results based on:	16,622,000 component test hours

Packaging Information

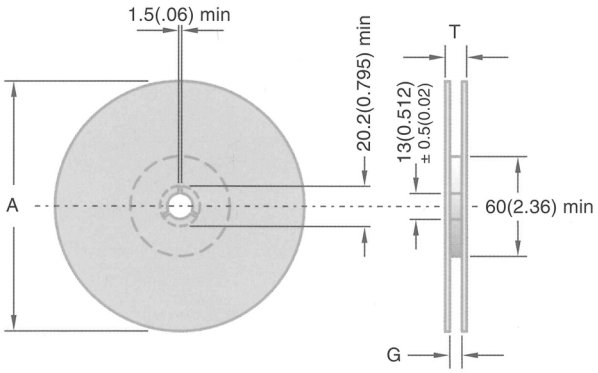
Tape and reel packing of surface mounting chip capacitors for automatic placement are in accordance with IEC60286-3.



Peel Force

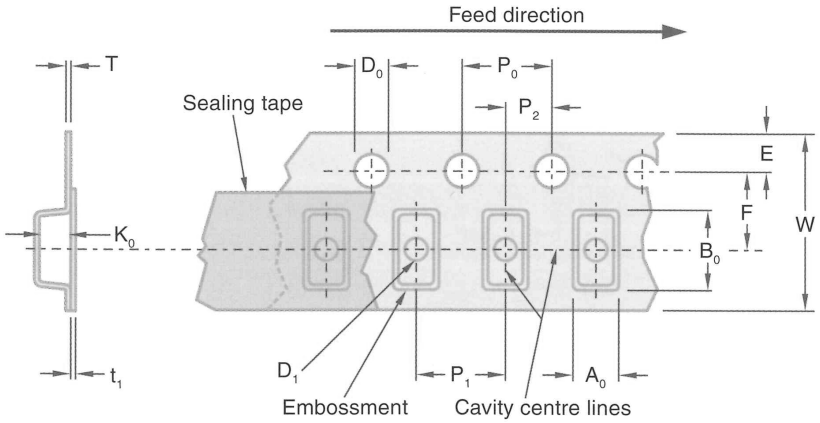
The peel force of the top sealing tape is between 0.2 and 1.0 Newton at 180°. The breaking force of the carrier and sealing tape in the direction of unreeling is greater than 10 Newton.

Reel Dimensions



Symbol	Description	178mm Reel	330mm Reel
A	Reel diameter	178 (7)	330 (13)
G	Reel inside width	8.4 (0.33)	12.4 (0.49)
T	Reel outside width	14.4 (0.56) max	18.4 (0.72) max

Tape Dimensions



		Dimensions mm (inches)	
Symbol	**Description**	**8mm Tape**	**12mm Tape**
A_0 B_0 K_0	Width of cavity Length of cavity Depth of cavity	Dependent on chip size to minimize rotation	
W	Width of tape	8.0 (0.315)	12.0 (0.472)
F	Distance between drive hole centres and cavity centres	3.5 (0.138)	5.5 (0.213)
E	Distance between drive hole centres and tape edge	1.75 (0.069)	
P_1	Distance between cavity centres	4.0 (0.156)	8.0 (0.315)
P_2	Axial distance between drive hole centres and cavity centres	2.0 (0.079)	
P_0	Axial distance between drive hole centres	4.0 (0.156)	
D_0	Drive hole diameter	1.5 (0.059)	
D_1	Diameter of cavity piercing	1.0 (0.039)	1.5 (0.059)
T	Carrier tape thickness	0.3 (0.012) ±0.1 (0.04)	0.4 (0.016) ±0.1 (0.04)
t_1	Top tape thickness	0.1 (0.004) max	

Packing Information

Missing Components

The number of missing components in the tape may not exceed 0.25% of the total quantity with not more than three consecutive components missing. This must be followed by at least six properly placed components

Identification

Each reel is labelled with the following information: manufacturer, chip size, capacitance, tolerance, rated voltage, dielectric type, batch number, date code and quantity of components.

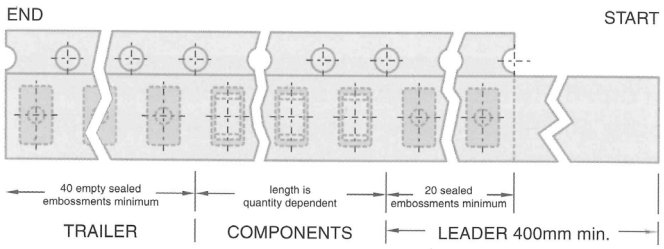
Component Orientation

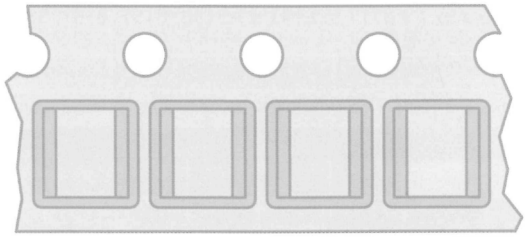
Tape and reeling is in accordance with IEC 60286 part 3, which defines the packaging specifications for leadless components on continuous tapes.

Notes: 1) IEC60286-3 states A0 <B0

2) Regarding the orientation of 1825 and 2225 components, the termination bands are right to left, NOT front to back. Please see diagram.

Leader Trailer



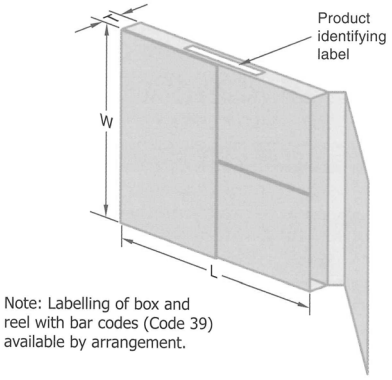


Orientation of 1825 & 2225 components

Outer Packaging

Outer carton dimensions mm (inches) max

Reel Size	No. of Reels	L	W	T
178 (7)	1	185 (7.28)	185 (7.28)	25 (0.98)
178 (7)	4	190 (7.48)	195 (7.76)	75 (2.95)
330 (13)	1	335 (13.19)	335 (13.19)	25 (0.98)



Note: Labelling of box and reel with bar codes (Code 39) available by arrangement.

Reel Quantities

Chip Size		0402	0505	0603	0805	1111	1206	1210	1410	1808	1812	1825	2211	2215	2220	2225
Max. Chip Thickness		0.5mm	1.3mm	0.8mm	1.3mm	2.0mm	1.6mm	2.0mm	2.0mm	2.0mm	2.5mm	2.5mm	2.5mm	2.5mm	2.5mm	2.5mm
		0.02”	0.05”	0.03”	0.05”	0.08”	0.06”	0.08”	0.08”	0.08”	0.1”	0.1”	0.1”	0.1”	0.1”	0.1”
Reel Quantities	178mm (7”)	10000	2500	4000	3000	1000	2500	2000	2000	1500	500	500	750	500	500	500
	330mm (13”)	15000	10000	16000	12000	5000	10000	8000	8000	6000	2000	2000	2000	2000	2000	2000

Notes:

1) The above quantities per reel are for the maximum manufactured chip thickness. Thinner chips can be taped in larger quantities per reel.

2) Where two different quantities are shown for the same case size, please contact the sales office to determine the exact quantity for any specific part number.

Bulk Packing – Tubs

Chips are supplied in rigid re-sealable plastic tubs together with impact cushioning wadding. Tubs are labelled with the details: chip size, capacitance, tolerance, rated voltage, dielectric type, batch number, date code and quantity of components.

Dimensions mm (inches)

H	60mm (2.36”)
D	50mm (1.97”)