NOVACAP

TECHNICAL BROCHURE

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A. INTRODUCTION

Ceramic chip capacitors are multilayer polycrystalline ceramic and metal composites, complex in their structure, behavior and application.

The purpose of the NOVACAP technical brochure is to provide the user of the product with basic information on the nature and properties of chip capacitors, their dielectric behavior, product classifications, test and quality standards, and information relevant to their applications. This fourth edition of the brochure contains new material pertaining to some of these topics, and has been prepared to satisfy the current changes in technology affecting the industry.

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B. CAPACITOR APPLICATIONS

Ceramic capacitor technology covers a wide range of product types, based on a multitude of dielectric materials and physical configurations, yet all are basically storage devices for electric energy which find use in varied applications in the electronic industry, and include the following:

Discharge of Stored Energy: This, the most basic of applications for a capacitor, involves the generation of a current pulse by discharge of a capacitor in the circuit.

Blockage of Direct Current: Capacitors, once charged, act as high impedance elements and thereby block the direct current in a specified portion of a circuit.

Coupling of Circuit Components: In an AC circuit, a capacitor charges and discharges with opposing polarity of the input signal, and thus allows alternating current to appear on either side of the component, so that sections of a circuit can be "coupled". The current does not flow physically through the capacitor, as the dielectric is an insulator; continuous current surges are the result of the change in voltage across the capacitor.

By-Passing of an AC Signal: By virtue of the ability of a capacitor to block direct current and yet permit the passage of alternating current, the device can be used in parallel with another circuit element to allow AC to "by-pass" the element without passing the DC portion of the signal.

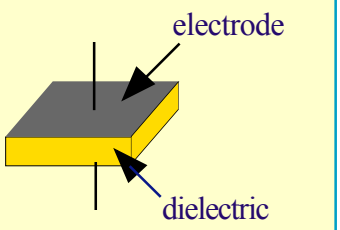
Frequency Discrimination: An input signal of mixed frequencies can be segregated by the use of a capacitor which is nonresponsive (by virtue of its capacitance value) to the low frequency portion of the signal. For capacitors in an AC circuit, the current "flow" increases with frequency. Also, the capacitance reactance, i.e. the resistance to flow of alternating current, is inversely proportional to the capacitance value. A device selected to display relatively minor opposition to current flow for the high frequency portion of the signal, while offering greater opposition to the lower frequency current, can thus be used to discriminate and filter out the desired frequency range.

Transient Voltage and Arc Suppression: Capacitors are utilized to stabilize circuits by removal of undesired transient voltage surges, and to eliminate arcing of contact points. The capacitor absorbs the energy generated by these voltage surges.

C. THE BASIC CAPACITOR

The basic model of a capacitor is a single plate device consisting of two conductors, or electrodes, separated by a dielectric material, as illustrated in Figure C-1. The dielectric must be an insulator material, the properties of which largely determine the electrical behavior of the device.

FIGURE C-1
SINGLE PLATE CAPACITOR



The dielectrics are characterized by their ability to store electrical charge (the dielectric constant) and their intrinsic responses to an electric field, namely capacitance change, loss characteristics, insulation resistance, dielectric strength, as well as the aging rate and the temperature dependence of these properties.

In general, capacitors utilize such dielectrics as air, (with a dielectric constant almost identical to a vacuum, and defined as 1) or naturally occurring dielectrics, such as mica, with a dielectric constant (K) of 4-8, or prepared materials, such as the ceramic groups, with K values ranging from K=9 to as high as K=18,000, as illustrated in Table C-1. Of the ceramic materials, those based on the titanates

TABLE C-1
DIELECTRIC CONSTANTS FOR VARIOUS MATERIALS

Vacuum:	1.0
Air:	1.004
Mylar:	3
Paper:	4-6
Mica:	4-8
Glass:	3.7-19
Alumina (Al_2O_3):	9
Titania (TiO_2):	85-170, (varies with crystal axis)
Barium Titanate ($BaTiO_3$):	1500
Formulated ceramics with discrete characteristics:	20-18,000

and niobates as the major constituent display the highest dielectric constant, can be formulated with suitable electrical characteristics, and are thus the basis of chip capacitor technology. All processes and other materials used in the manufacture of chip capacitors are oriented towards optimization of the electrical properties of these dielectrics.

D. CAPACITANCE

The principal characteristic of a capacitor is that it can store an electric charge (Q), which is directly proportional to the capacitance value (C) and the voltage applied (V).

$$Q = CV$$

The charging current I is therefore defined as

$$I = dQ/dt = CdV/dt.$$

The value of capacitance is defined as one Farad when the voltage across the capacitor is one volt, and a charging current of one ampere flows for one second.

$$C = Q/V = \text{Coulomb/Volt} = \text{Farad}$$

Because the Farad is a very large unit of measurement, and is not encountered in practical applications, fractions of the Farad are commonly used, namely:

picofarad (pF)	$= 10^{-12}$ Farad
nanofarad (nF)	$= 10^{-9}$ Farad
microfarad (mF)	$= 10^{-6}$ Farad

E. FACTORS AFFECTING CAPACITANCE

For any given voltage the capacitance value of the single plate device of Figure C-1 is directly proportional to the geometry and dielectric constant of the device:

$$C = KA/f(t)$$

K = dielectric constant
A = area of electrode
t = thickness of dielectric
f = conversion factor

In the English system of units, f=4.452, and using dimensions in inches for A and t, the capacitance value is expressed in picofarads (pF). For example: for a device as in Figure C-1, with a 1.0 X 1.0" area, .056" dielectric thickness, and a dielectric constant of 2500,

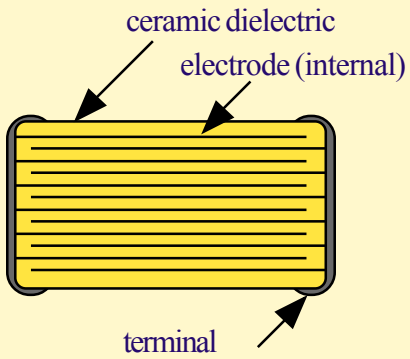
C = 2500 (1.0)(1.0)/4.452 (.056) = 10,027 pF

utilizing the Metric System, the conversion factor is f= 11.31, and dimensions are in centimeters.

C = 2500 (2.54)(2.54)/11.31 (.1422) = 10,028 pF.

As is evident from the above relationship of capacitance to geometry, greater capacitance can be achieved by increasing the electrode area while decreasing the dielectric thickness. As it is physically impractical to increase area in a single plate device with thinner dielectric, the concept of stacking capacitors in a parallel array was conceived to produce a physically sound device with more capacitance per unit volume, as illustrated in Figure E -1.

FIGURE E-1
MULTILAYER CAPACITOR



In this "multilayer" configuration, the area A is increased by virtue of many electrodes in parallel arrangement, in a construction permitting very thin dielectric thickness between opposing electrodes, such that the capacitance C is enlarged by the factor N (number of dielectric layers) and reduced dielectric thickness t', where A' is now the area of overlap of opposing electrodes:

$$C = KA'N/4.4452(t')$$

The capacitance value previously obtained for the inch square by 056" single plate device can now be produced with the same dielectric in a multilayer unit of only .050" x .050" x .040" dimensions and thirty (30) dielectric layers of thickness .001" (where A', the electrode overlap, is .030 x .020").

$$C = 2500\ (.030)\ (.020)\ 30/4.452\ (.001) = 10{,}107\ pf$$

This example, in effect, shows that multilayer construction can deliver the same capacitance in a volume 700 times smaller than that of the single plate device. Chip capacitors are therefore designed and manufactured to maximize the volumetric efficiency of capacitance, by optimizing the geometry and by the selection of dielectric formulations with high dielectric constant and general electrical properties, namely good insulation resistance and dielectric strength, which permit very thin layer construction.

F. DIELECTRIC BEHAVIOR

Dielectric behavior occurs in all insulators - solids, liquids and gases, yet it is not yet fully understood, and certain generalizations apply, especially when considering aggregates, such as the polycrystalline ceramics.

DIELECTRIC POLARIZATION

Dielectric polarization arises due to the existence of atomic and molecular forces, and appears whenever charges in a material are somewhat displaced with respect to one another under the influence of an electric field.

In a capacitor, the negative charges within the dielectric are displaced toward the positive electrode, while the positive charges shift in the opposite direction. As charges are not free to move in an insulator, restoring forces are activated which either do work, or cause work to be done on the system, i.e. energy is transferred. On charging a capacitor, the polarization effect opposing the applied field draws charges onto the electrodes, storing energy. On discharge, this energy is released.

A result of the above interaction is that certain materials, which possess easily polarizable charges, will greatly influence the degree of charge which can be stored in a capacitor. The proportional increase in storage ability of a dielectric with respect to a vacuum is defined as the dielectric constant of the material.

The degree of polarization P is related to the dielectric constant K, and the electric field strength E as follows:

$P = e_o (K-1) E$

where e_o is the permittivity of free space, (a constant).

The total polarization of a dielectric arises from four sources of charge displacement: (a) electronic displacement, (b) ionic displacement, (c) orientation of permanent dipoles and (d) space charge displacement. The total contribution of polarization to the dielectric constant is therefore a summation of the above:

$Pt = Pe+Pi+Pd+Ps$

Electronic Displacement: This effect is common to all materials, as it involves distortion of the center of charge symmetry of the basic atom. Under the influence of an applied field, the nucleus of an atom and the negative charge center of the electrons shift, creating a small dipole. This polarization effect is small, despite the vast number of atoms within the material, because the moment arm of the dipoles is very short, perhaps only a small fraction of an Angstrom ($1Å = 10^{-10}$ meters).

Ionic Polarization: Ionic displacement is common in ceramic materials, which consist of crystal lattices occupied by cations and anions. Under the influence of an electric field, dipole moments are created by the shifting of these ions towards their respective (opposite) polarity of the field. The displacement, or moment arm of the dipoles can be relatively large in comparison to the electronic displacement, (although still much less than one Angstrom unit), and therefore can give rise to high dielectric constants in some ceramics.

Dipole Orientation: This is a phenomenon involving rotation of permanent dipoles under an applied field. Although permanent dipoles exist in ceramic compounds, such as in SiO_2, which has no center of symmetry for positive and negative charges, dipole orientation is not found to occur, as the dipole is restricted from shifting by the rigid crystal lattice; reorientation of the dipole is precluded as destruction of the lattice would ensue. Dipole orientation is more common in polymers which by virtue of their atomic structure permit reorientation. Note that this mechanism of permanent dipoles is not the same as that of induced dipoles of ionic polarization.

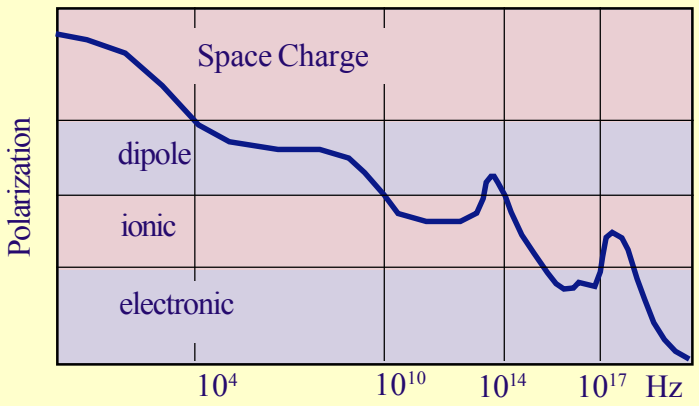
Space Charge Polarization: This mechanism is extrinsic to any crystal lattice. The phenomenon arises due to charges which exist due to contaminants or irregular geometry of the interfaces of polycrystalline ceramics, and is therefore an extraneous contribution. These charges are partly mobile and migrate under an applied field.

EFFECT OF FREQUENCY ON POLARIZATION

The mechanisms of polarization have varying time response capability to an applied field frequency, and the net contribution of polarization to the dielectric constant is therefore frequency dependent. Electronic displacement responds rapidly to the field reversals, and no lag of the polarization contribution occurs up to 10^{17} Hz. As is expected, ions, which are larger and must shift within the crystal structure, are less mobile, and have a less rapid response. The polarization effect of ionic displacement decreases at 10^{13} Hz. At this frequency, the ionic displacement begins to lag the field reversals, increasing the loss factor and contributing less to the dielectric constant. At higher frequency, the field reversals are such that the ions no longer "see" the field (the natural frequency of ions is less than the applied frequency), and no polarization (or loss factor) contribution is made by ionic displacement.

Dipole orientation and space charge polarization have slower frequency responses. The total net effect is illustrated in Figure F-1. The peaks which occur near the limiting frequency for ionic and electronic polarization are due to the resonance points, where the applied frequency equals the natural frequency of the material

FIGURE F-1
POLARIZATION VS. FREQUENCY



(from W. D. Kingery, Introduction to Ceramics)

The variation with frequency of the polarization mechanisms is reflected when measuring dielectric constant of a capacitor. As expected, capacitance value, i.e. dielectric constant, always decreases with increased frequency, for all ceramic materials, although with varying degrees, depending upon which type of polarization mechanism is dominant in any particular dielectric type.

DIELECTRIC LOSS

In an AC circuit, the voltage and current across an "ideal" capacitor are 90° out of phase. This is evident from the following relationships:

$$Q = CV$$

For an alternating applied field,

$$V = Vo \sin \omega t$$

where Vo is the amplitude of the sinusoidal signal, and ω is the frequency.

Therefore

$$Q = CVo \sin \omega t$$

The current

$$I = dQ/dt = d/dT\ CVo \sin \omega t$$

Therefore

$$I = CVo\ \omega \cos \omega t$$

Because

$$\cos \omega t = \sin (\omega t + 90^{o})$$

the current flow is therefore 90° out of phase with the voltage. Real dielectrics, however, are not perfect devices, as the resistivity of the material is not infinite, and the lag or "relaxation time" of the polarization mechanisms with frequency generates losses.

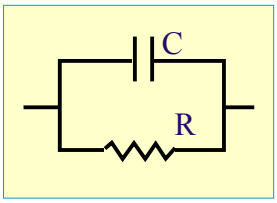
The above model for an "ideal" capacitor, in practical applications, must be modified; a practical model for a real capacitor can be considered to be an ideal capacitor in parallel with an ideal resistor.

Again, for the capacitor, the voltage

$$V = Vo \sin \omega t$$

in an alternating field, and

$$Ic = CVo\ \omega \cos \omega t$$



For the ideal resistor

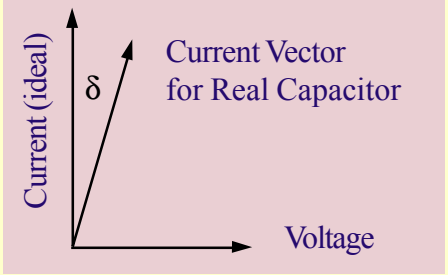
$$Ir = V/R = Vo/R \text{ Sin } \omega t$$

The net current flow is therefore

$$Ic + Ir = Inet = CVo\ \omega \text{ Cos } \omega t + Vo/R \text{ Sin } \omega t$$

The two portions of the current flow indicate that some current (that contributed by the resistive portion of the capacitor) will not be 90° out of phase with the voltage. The angle by which the current is out of phase from ideal can be determined, and the tangent of this angle is defined as the loss tangent or dissipation factor, as illustrated in Figure F-2:

FIGURE F-2
LOSS TANGENT IN REAL CAPACITOR



The loss tangent, Tan δ, is a material property, and is not dependent on geometry of a capacitor. The loss tangent greatly influences the usefulness of a dielectric in electronic applications. In practice it is found that lower dissipation factor is associated with materials of lower dielectric constant. Higher K materials, which develop this property by virtue of high polarization mechanisms, display higher dissipation factor.

EFFECT OF FREQUENCY ON DIELECTRIC LOSS

As was illustrated in paragraph F-2, the frequency at which a dielectric is used has an important effect on the polarization mechanisms, notably the "relaxation" process or time lag displayed by the material in following field reversals in an alternating circuit. Low relaxation time is associated with instantaneous polarization processes, large relaxation time with delayed polarization processes. Ceramic dielectrics consist of atoms and ions, the latter which contribute largely to the dielectric losses. The loss contribution is maximized at a frequency where the applied field has the same period of the relaxation process. To state the matter simply, losses are small when the relaxation

time and period of the applied field differ greatly:

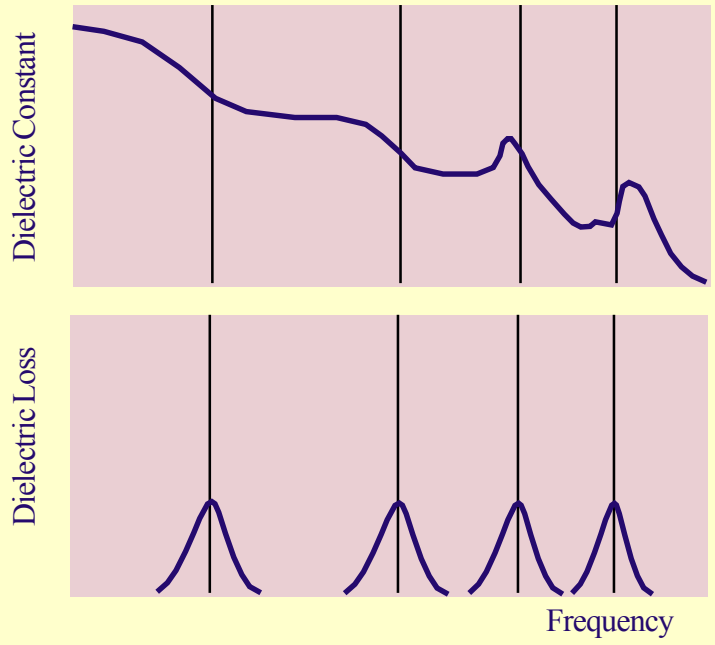
a) relaxation time >> field frequency, loss is small
b) relaxation time << field frequency, loss is small
c) relaxation time = field frequency, loss is maximized

Situation (a) generates little loss, as the polarization mechanism is much slower than the field reversals, and the ions cannot follow the field at all, hence creating no heat loss. The inverse occurs in situation (b), where the polarizing processes can easily follow the field frequency, with no lag. In case (c), however, ions can follow the field, but limited by their relaxation time, and thus generating the highest loss with frequency.

Ceramic dielectric formulations always show a range of relaxation times over the frequency spectrum, as these materials consist of polycrystalline matter. The variation of dielectric loss with frequency coincides with the change in dielectric constant, as the two are related to the polarizing mechanisms, as shown in Figure F-3. In high frequency applications, a figure of merit known as the "Q factor" is often used, which is the reciprocal of the loss tangent:

$$Q = 1 / \tan \delta$$

FIGURE F - 3
RELAXATION EFFECTS ON DIELECTRIC CONSTANT AND DIELECTRIC LOSS



G. DIELECTRIC PROPERTIES

There are additional electrical properties characteristic of dielectrics which greatly determine the merit of performance of these materials in capacitor applications.

INSULATION RESISTANCE

The insulation resistance is a measure of the capability of a material to withstand leakage of current under a Vdc potential gradient.

Insulators are materials that have no free electrons in their atomic structure which are free to move under any applied field intensity. In ceramic dielectrics, the electrons are tied up in ionic and covalent bonding of the atoms, and by definition these materials should possess almost infinite electrical resistivity. In reality, however, insulators do not display infinite but limited resistivity, as there are impurities and defects in the atomic lattice structure which give rise to charge carriers.

In oxide ceramics, such as the titanates, charge carriers can arise due to imperfect stoichiometry, i.e. the ratio of anions to cations is not charge balanced, and the crystal lattice of the material will have vacant lattice sites (holes) and interstitial ions. These imperfections can occur due to impurities which substitute other cations without satisfying the charge balance. For example, an Al^{3+} cation replaces a Ti^{4+} cation, leaving a net negative charge. Also, the ratio of oxygen to other ions may be insufficient to maintain ideal valency, creating a net positive charge. The latter can easily occur if the partial pressure of oxygen during firing of the material is insufficient and a “reduction” condition exists. Severe reduction, in fact, will lower the resistivity of the titanates to the point where semiconductor properties become evident.

The interstitial ions resulting from the above have a definite random mobility, which is temperature dependent; ion diffusion increases with temperature as the added thermal energy overcomes the energy barriers for diffusion. Under an applied field, diffusion is no longer random, but along the potential gradient of the field, generating a leakage current.

The insulation resistance of chip capacitors is therefore dependent on formulation, processing (firing) and temperature at measurement. In all dielectrics, the resistivity decreases with temperature, and a considerable drop is observed from the low (-55°C) to the high (125°C) range of the MIL temperature specification.

An important consideration when measuring the insulation resistance of capacitors is the relationship between IR and the capacitance value of the unit under test. It follows that the capacitance value is inversely proportional to the insulation resistance, i.e., higher value units display lower insulation resistance. The reason for this behavior is that capacitance and leakage current are di-

rectly proportional to one another, as can be demonstrated using Ohm's Law and the relationship of capacitance to geometry: Ohm's Law states that the current (I) in a conductor is related to the applied voltage (V) and the resistance (R) of the conductor as:

$$I = V/R$$

The resistance (R), however, is a dimensionally dependent property, and is related to the intrinsic resistivity of the material (p) as follows:

$$R = pL/A$$

where L = the length of the conductor
A = the cross sectional area of the conductor

The current (I), therefore, can be expressed as:

$$I = VA/pL$$

When considering a ceramic capacitor, the leakage current (i) through the insulator can be expressed as in the above formula:

$$i = VA'/pt$$

where V = test voltage
A'= active electrode area
p = dielectric resistivity
t = dielectric thickness

As is evident from the above relationship, for any given test voltage (V), the leakage current is directly proportional to the active electrode area of the capacitor, and is inversely proportional to the thickness (and resistivity) of the dielectric layer, i.e.,

$$i \propto A'/t$$

Similarly, the capacitance (C) is directly proportional to the active electrode area, and inversely proportional to the dielectric thickness, for

$$C = KA'/4.452\ t, \text{ where}$$

K = dielectric constant
A' = Active electrode area
t = dielectric thickness

Hence

$$C \alpha A'/t, \text{ and } i \alpha C$$

The leakage current (i) is the inverse of the insulation resistance, such that:

$$IR \alpha 1/C$$

Based on the above, certain obvious generalizations apply:

The insulation resistance is a function of the test voltage, as leakage current is directly proportional to the applied voltage:

$$i = VA'/pt, \text{ or } I\,R = pt/VA'$$

For any given capacitor, the insulation resistance is largely dependent on the resistivity (p) of the dielectric, which is a property of the material, dependent on formulation, and temperature of measurement, as described previously.

The measured IR is inversely proportional to the capacitance value of the unit under test, i.e., IR is a function of capacitance, and hence minimum standards for IR in the industry are established as the product of the resistance (R) and the capacitance (C), (RxC), as shown in Table G-1. EIA specifications require that the RxC product exceed 1000 Ohm-Farad (often expressed as 1000 Megohm-Microfarad) at 25°C, and 100 Ohm-Farad at 125°C, (10% of the values of Table G-1).

Dielectrics normally have very high electrical resistance and measurements are reported in large multiples of the Ohm:

1 Tera-ohm (TΩ) = 10^{12} Ohm
1 Giga-ohm (GΩ) = 10^{9} Ohm
1 Mega-ohm (MΩ) = 10^{6} Ohm

In addition to the material and geometric variables, there are other physical factors which influence the insulation resistance of capacitors.

Surface Resistivity: The surface of the dielectric may possess different resistivity than the bulk material, due to absorbed impurities, or water moisture.

Defects: Dielectric formulations are polycrystalline ceramic aggregates, containing grain

boundaries and pore volume in their microstructure which decrease the intrinsic resistivity of the material. Statistically, the occurrence of these physical defects is directly proportional to chip volume and the complexity of its structure. It follows therefore that larger units, or larger electrode plate area and more numerous electrode layers, may possess a lower resistivity and thus lower insulation resistance than predicted for smaller devices.

TABLE G-1
MINIMUM IR STANDARDS VS. CAPACITANCE

Capacitance	Min IR (GΩ)	Min RxC (ΩF) @ 25°C
0.1 pF to .010 µF	100.00	1000
.015	66.67	
.022	45.45	
.033	30.30	
.047	21.28	
.068	14.71	
.100	10.00	
.150	6.67	
.220	4.55	
.330	3.03	
.470	2.13	
.680	1.47	
1.00	1.00	
etc.	etc.	

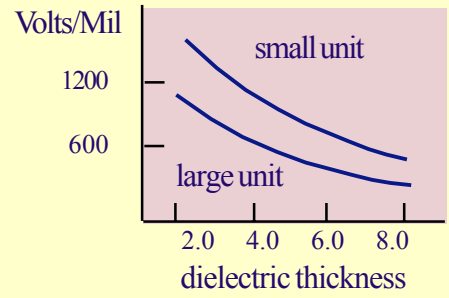
DIELECTRIC STRENGTH

The dielectric strength is a measure of the ability of the material to withstand a large field strength without electrical breakdown, and is usually expressed in volts per mil (.001') or volts per cm of dielectric.

Dielectric failure occurs in insulators when the applied field reaches a threshold point where the restoring forces within the crystal lattice are overcome and a field emission of electrons occurs, generating sufficient number of free electrons which on collision create an avalanche effect and results in a sudden burst of current which punctures the dielectric. In addition to this electric type of failure, high voltage stress creates heat, which lowers the resistivity of the material to the point, where, with sufficient time, a leakage path may develop through the weakest portion of the dielectric. This type of thermal failure is of course temperature dependent, and dielectric strength decreases with temperature.

The intrinsic dielectric strength of any insulator is diminished by physical defects in the microstructure of the material, and, as with insulation resistance, a dependency on geometry is observed with actual measurements. Dielectric strength is inversely proportional to dielectric thickness, as increased volume of the material increases the probability of random defects, as illustrated in Figure G-1.

FIGURE G - 1
DIELECTRIC STRENGTH VS. DIELECTRIC THICKNESS



Similarly, dielectric strength is inversely proportional to the electrode layer count of a chip capacitor and to its physical size.

Chip capacitors are designed with a margin of safety based on the above considerations, to preclude failure in use and at the dielectric withstanding voltage test, which typically is 2.5 times the working voltage of the device.

AGING

Ceramic capacitors made with ferroelectric formulations display a decay of capacitance and dielectric loss with time. This phenomenon, called aging, is reversible and occurs due to the crystallographic changes of ferroelectrics with temperature.

The ferroelectric group of dielectrics is based on barium titanate ($BaTiO_3$) as the main constituent, an oxide which undergoes changes in crystal habit or symmetry that give rise to ferroelectric domains. At the Curie Temperature of 120°C, $BaTiO_3$ transforms from a tetragonal to a cubic crystal habit, and spontaneous polarization no longer occurs. On cooling through and below the Curie point, the material again transforms from a cubic to a tetragonal crystal configuration in which the lattice has no center of symmetry and the Ti^{4+} cation can occupy one of two asymmetrical sites, giving rise to a permanent electric dipole. These dipoles form spontaneously and are somewhat ordered, as adjacent unit cells influence one another sufficiently to interact and create domains of

similar polarity. The domains of parallel electrical polarity are random in orientation (without the influence of an electric field) and impart a certain strain energy to the system. The relaxation of this strain energy is attributed to be the mechanism of aging of the dielectric constant, and is found to have the following relationship with time:

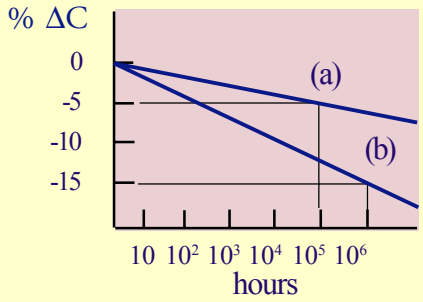
$$K = K_o - m \log t$$

where K = dielectric constant at any time t
Ko = dielectric constant at time t,(t_o<t)
m = rate of decay

The above relationship is logarithmic, and data will approximate a straight line when plotted on semilog paper as illustrated in Figure G-2. The percent change of K (or capacitance) per decade can be calculated and used as a figure of merit for dielectric formulations.

The microstructure details which affect polarization (material purity, grain size, sintering, grain boundaries, porosity, internal stresses) also determine freedom of domain wall movement and reorientation, and it is found that the aging rate is composition and process dependent and is sensitive to variables which also influence the dielectric constant of the material.

FIGURE G -2
FERROELECTRIC AGING



Example (a) Aging Rate = -5% / 5 decades = 1.0%/decade hr.
Example (b) Aging Rate = -15% / 6 decades = 2.5%/decade hr.

The loss of capacitance with time is unavoidable with ferroelectric formulations, although it can be reversed by heating the dielectric above the Curie Point and reverting the material back to a "paraelectric" cubic state. On cooling, however, spontaneous polarization will again occur as the material transforms to the tetragonal crystal habit, and new domains recommence the aging process.

As is expected, no aging is observed only in paraelectric formulations, such as NPO, which do not possess the mechanism of spontaneous polarization. The rate at which aging may occur can be influenced by "voltage conditioning" of capacitors. It is found that units stressed by a dc voltage at elevated temperature (below the Curie Point) will experience a loss of capacitance, but with a consequently lower aging rate. It is theorized that the voltage stress at the elevated temperature accelerates the domain relaxation process. This voltage conditioning effect is, of course, eliminated if the unit ever experiences temperatures exceeding the Curie Point.

Capacitor manufacturers compensate for capacitance loss of ferroelectric dielectrics by adjustment of the testing limits, such that units do not age out of tolerance over a long time period. For example, for a dielectric with a 1.5%/decade aging rate, the testing limits are raised 3%, i.e. two decades of time. Units tested 100 hours after last exposure to the Curie Temperature therefore will remain within tolerance for another two decades or 10,000 hours.

ELECTRO-MECHANICAL COUPLING

Dielectric materials always display an elastic deformation when stressed by an electric field, due to displacements of ions within the crystal lattice. The mechanism of polarization, i.e. the shifting of ions in the direction of an applied field, results in a constriction of surrounding ions in the atomic lattice, as restoring forces between atoms strive to balance the system. This behavior is called electrostriction, and is common to all crystals endowed with a center of symmetry. Electrostriction is a one-sided relationship, in that an electric field causes deformation, but an applied mechanical stress does not induce an electric field, as charged centers are not displaced.

Piezoelectric materials are those which display a two-sided relationship of mechanical stress and polarization, which is attributed to crystal lattice configurations which lack a center of symmetry. Upon compression, the centers of charge shift and produce a dipole moment, resulting in polarization. This effect is a true linear coupling, as the elastic strain observed is directly proportional to the applied field intensity, and the polarization obtained is directly proportional to the applied mechanical stress.

As explained previously in paragraph G-3, barium titanate, the major constituent of ferroelectric dielectrics, lacks a center of symmetry in the crystal lattice at temperatures below the Curie Point (120°C). The material therefore is piezoelectric in nature. When heated past the Curie Temperature, the crystal lattice changes from the tetragonal to the cubic configuration, which possesses a center of symmetry and piezoelectric effects are no longer observed.

DIELECTRIC ABSORPTION

Dielectric absorption is the measurement of a residual charge on a capacitor after discharge, and is expressed as the percent ratio of the residual voltage to the initial charge voltage.

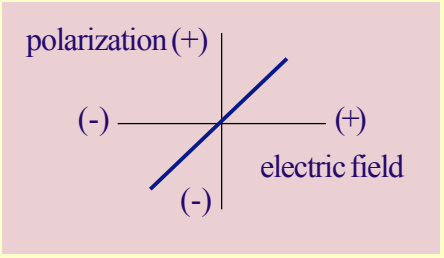
The residual voltage, or charge, is attributed to the relaxation phenomena of polarization. As explained in paragraph F-2, the polarization mechanisms can lag the applied field. The inverse situation, whereby there is a lag on depolarization, or discharge, also applies. A small fraction of the polarization, in fact, may persist after discharge for long time periods, and can be measured on the device with a high impedance voltmeter.

Dielectrics with higher dielectric constant, and, therefore more polarizing mechanisms, typically display more dielectric absorption than lower K materials.

H. FERROELECTRIC CERAMICS

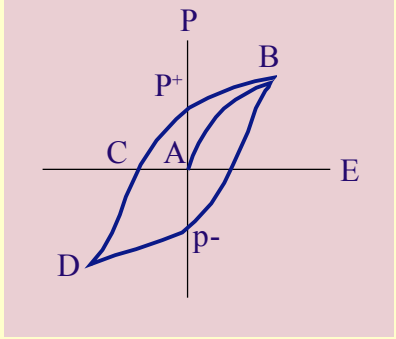
Ferroelectric dielectrics differ from the "paraelectric" materials in that a nonlinear response of charge or polarization versus voltage occurs due to the crystal structure of the material. Ionic displacements in paraelectric ceramics, such as TiO_2, are totally reversible, as ions return to their original position once an applied field is removed, and the polarization effect is linear as depicted in Figure H-1.

FIGURE H - 1
POLARIZATION OF LINEAR DIELECTRIC



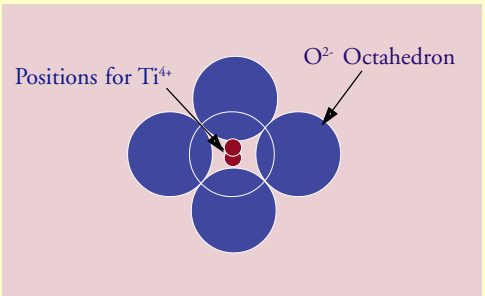
Ferroelectric ceramics are those which display a hysteresis effect of polarization with an applied field, as shown in Figure H-2. The hysteresis loop is caused by the existence of permanent electric dipoles in certain materials, (such as barium titanate), which develop spontaneously below the Curie

FIGURE H -2
FERROELECTRIC HYSTERESIS



Temperature, as explained in paragraph G-3. These dipoles arise due to the fact that in the tetragonal unit cell of $BaTiO_3$, the Ti^{4+} cation is surrounded by Six O^{-2} anions in a slightly deformed octahedral configuration, and can occupy one of two asymmetrical sites, as illustrated in Figure H-3. In either position, the Ti^{4+} cation is not coincident with the negative charge center of the oxygen anions by a small fraction of an Angstrom, creating an electric dipole. The energy barrier between the two possible Ti atom positions is sufficiently low to permit motion of the atom between sites by the coercion of an electric field, and the material can thus be directionally polarized with ease. The interaction between adjacent unit cells, in fact, is sufficient to create domains of parallel polarity the instant the material assumes its ferroelectric state on cooling through the Curie Point.

FIGURE H - 3
Ti^{4+} CATION IN THE O^{2-} OCTAHEDRON

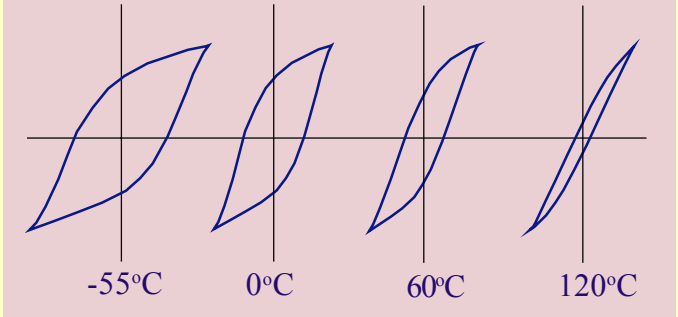


Upon creation, the ferroelectric domains are random in orientation, and the material has no polarization. In reference to Figure H-2, this state is equivalent to point A. If an external field is now applied, Ti atoms become displaced in the direction of the field, such that domains more favorably

aligned with the field will grow, at the expense of those which are not, creating a rapid and major polarizing effect until a maximum orientation with the field is achieved (point B). Removal of the field at this point will eliminate any normal ionic polarization, but as is evident from the model of Figure H-3, the Ti atoms remain in their now oriented sites, and a remnant polarization (P+) isobserved. In order to remove this polarization it becomes necessary to apply an opposing field (point C) which reverts half the volume of the domains to favor the new field direction. Continuation of the field cycle inverts the polarization to a maximum (at point D) and removal of the negative field leaves a net polarization (P-). Further cycles of the electric field retrace the original path, creating a continuous hysteresis effect. A condition of zero polarization at 0 volts (point A) can only be again achieved by short circuiting the capacitor and heating past the Curie Point to generate a new system of random ferroelectric domains. Ferroelectric domains can actually be observed in polycrystalline barium titanate, where etched polished surfaces reveal differences in orientation on the grain structure of the material.

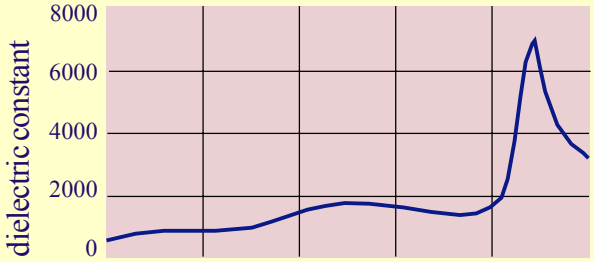
The ferroelectric hysteresis loop varies in shape with temperature. At lower temperatures there is less thermal motion of atoms and a greater field is required to orient the domains. Measurements at higher temperatures show that the coercive field required for polarization decreases, until at the Curie Temperature the hysteresis effect disappears and linearity is approximated (Figure H-4).

FIGURE H-4
HYSTERESIS LOOP AT VARIOUS TEMPERATURES



It should be noted that barium titanate undergoes other phase transformations below the Curie Point, which are accompanied by changes in the dielectric constant of the ceramic. In addition to the cubic to tetragonal transformation on cooling through the 120˚C Curie Point, a change from tetragonal to orthorhombic occurs at 0˚C, which then transforms to the rhombohedral crystal habit at -90˚C. The variation of the relative dielectric constant with temperature is illustrated in Figure H-5.

FIGURE H - 5
TEMPERATURE COEFFICIENT FOR $BaTiO_3$



The variations of electrical properties of $BaTiO_3$, in addition to the changes of these with temperature, present some obvious problems. The polarization obtained is a function of the electric field intensity, due to the energy required for domain orientation, i.e. K is a function of the applied field. In addition, the dielectric constant is highly temperature dependent and practical applications specify stability over a -55˚C to 125˚C temperature range. Also, as indicated previously, ferroelectric ceramics display aging and piezoelectric effects.

There are, fortunately, other elements which can be incorporated into the $BaTiO_3$ perovskite crystal structure to modify its properties. Lead titanate, for example, which also has a perovskite structure, readily forms solid solutions with $BaTiO_3$, i.e. the Pb^{2+} cation can substitute the Ba^{2+} cation. Other partial substitutions for Ba^{2+}, (such as Sr^{2+}, Cd^{2+} and Ca^{2+}), as well as replacement in part for the Ti^{4+} cation (by Sn^{4+}, Zr^{4+}, and Hf^{4+}) are also used to modify the dielectric behavior and temperature dependence of $BaTiO_3$. These additives greatly enhance the range of compositions and possible dielectric characteristics, and much effort has been expended in recent years to optimize these materials for practical applications.

Specifically, additives are utilized to shift the Curie Point such that the high K properties of the ferroelectric can be put to work at or near room temperature. Examples of such materials are $SrTiO_3$ and $CaZrO_3$. Other materials may transfer the Curie Point to more elevated temperatures ($PbTiO_3$). In addition to "shifter" additives, materials which depress the dielectric constant peak at the Curie Point are utilized, to provide a more stable K value over temperature. These compositional additives are call "depressors," examples of which are $MgZrO_3$ and $Bi_2Sn_3O_9$. These materials are thus used in careful proportions to maximize the usefulness of the dielectric over the practical temperature range, i.e. the high K Curie peak is "shifted" towards room temperature, and the spike effect is depressed to provide a reasonable capacitance temperature coefficient. In polycrystalline ceramics many individual crystal characteristics can be combined which mask one another to

provide relatively stable characteristics.

Additions which do not form a solid solution, or only a partial solid solution with the host material, also affect the microstructure, by providing a second intergranular phase. Grain boundary phases which are not ferroelectric greatly affect the electrical properties of the composite, as these phases somewhat isolate the ferroelectric grains and thus inhibit domain interaction, depressing the dielectric constant, aging rate and the piezoelectric effects.

In addition to the purposes described above, other ingredients are used to aid in fabrication of the multilayer capacitor, such as additives which flux the ceramic to permit sintering at lower and more reasonable temperature or inhibit excessive grain growth and provide denser microstructure. Often, minor percentages of certain oxides will determine other electrical properties, such as insulation resistance at 25°C, or at 125°C, or dielectric strength.

I. LINEAR DIELECTRICS

Dielectrics which are non-ferroelectric show a linear relationship of polarization to voltage (Figure H-1) and are formulated to have a linear temperature coefficient. These materials consist primarily of TiO_2 and therefore exhibit lower dielectric constant (<150) but more importantly, also lower dielectric loss and no aging of capacitance with time. These properties, along with negligible dependence of capacitance with voltage or frequency, make these dielectrics useful in capacitor applications where close tolerance and stability are required.

Linear dielectrics are also referred to as Temperature Compensating, as the temperature coefficient can be modified to give predictable slopes of the temperature coefficient (T.C.) over the standard -55°C to 125°C range. These slopes vary from approximately a positive of 100 parts per million per degree C (ppm/ °C) to a slope of typically negative 750ppm/ °C. These values are reported as P100 or N750 respectively. A flat slope, which is neither positive nor negative is a negative-positive-zero (NPO or COG) and is one of the most common of all dielectric characteristics.

A series of linear dielectrics known as the extended T.C. type, range from N750 to as negative as N5600. These values are obtained by using dielectrics with the Curie Point well below the -55°C lower limit of the MIL Specifications, such that the T.C. portion between -55°C to 125°C is approximately linear.

J. CLASSES OF DIELECTRICS

Dielectric formulations are identified and classified in the industry by the capacitance temperature coefficient of materials. Two basic groups (Class I and Class II) are used in the manufacture of ceramic chip capacitors. A third (Class III) identifies the reduced barium titanate barrier-layer formulations utilized in the production of disc capacitors.

The temperature coefficients are determined by measurement of the capacitance change at various temperatures from reference room temperature (25°C), using an environmental chamber. The temperature coefficient (T.C.) is expressed as the percent capacitance change (%ΔC) or parts per million per degree C (ppm/°C) change from reference. The T.C. characteristic is usually illustrated graphically over the standard EIA and MIL temperature ranges (-55°C to 85°C, and -55°C to 125°C respectively). The method of calculation of the temperature coefficient is described in Section K-1.

Class I Dielectrics

This group identifies the linear dielectrics described in Section 1. These materials display the most stable characteristics, as they are non-ferroelectric (paraelectric) formulations, based mostly on TiO_2, with dielectric constants under 150. The "extended" temperature compensating ceramics are a subgroup of formulations which utilize small additions of other (ferroelectric) oxides, such as $CaTiO_3$ or $SrTiO_3$ and which display near-linear and predictable temperature characteristics with dielectric constants ranging up to 500. Both categories are used in circuitry requiring stability of the capacitor, i.e. negligible or no aging of the dielectric constant, low loss (DF<.001, or <.002 for the extended T.C. bodies), negligible or no change in capacitance or dielectric loss with voltage or frequency, and predictable linear behavior with temperature within prescribed tolerances.

A letter-number-letter code which defines the temperature coefficients of Class I dielectrics has been developed and is defined in the Electronic Industries Association (EIA) Standard 198, as shown in Table J-1.

The most common Class I dielectric for chip capacitors is the COG designation, i.e. 0 ppm/°C ±30 ppm/°C temperature coefficient, which is the NPO (negative-positive-zero) MIL specification, for flat temperature coefficient.

TABLE J - 1
EIA DESIGNATIONS FOR CLASS I DIELECTRICS

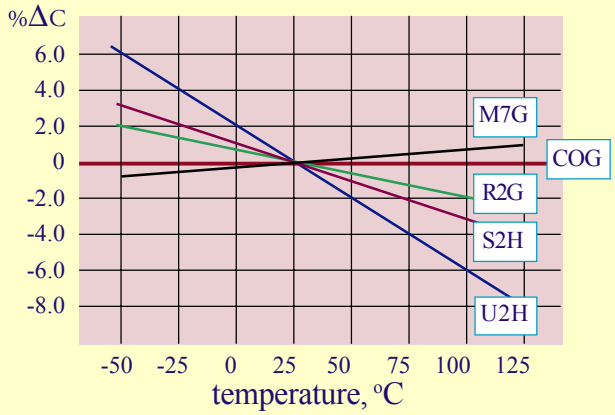
(a) significant figure of temp. coeff. of capacitance (ppm/°C)	(b) letter code for (a)	(c) multiplier applicable to column (a)	(d) numerical codes for column (c)	(e) tolerance of temp. coeff. (ppm/°C)	(f) letter code for column (e)
0.0	C	-1.0	0	30	G
1.0	M	-10	1	60	H
1.5	P	-100	2	120	J
2.2	R	-1000	3	250	K
3.3	S	-10000	4	500	L
4.7	T	+1	5	1000	M
7.5	U	+10	6	2500	N
		+100	7		
		+1000	8		
		+10000	9		

Some examples from Table J-1:

R2G	Negative	220 ppm/°C	±30 ppm/°C	(N220)
S2H	Negative	330 ppm/°C	±60 ppm/°C	(N330)
U2H	Negative	750 ppm/°C	±60 ppm/°C	(N750)
M7G	Positive	100 ppm/°C	±30 ppm/°C	(P100)

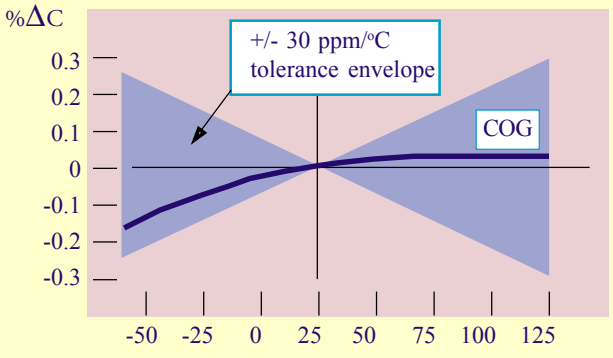
Some of the above examples are illustrated graphically in Figure J-1.

FIGURE J - 1
T. C. OF LINEAR DIELECTRICS



Actual measurements of temperature coefficient may not necessarily be perfectly linear, but are acceptable if the data fall within the permissible tolerance limits specified by the last letter of the EIA code, as illustrated for COG dielectric in Figure J-2.

FIGURE J - 2
TOLERANCE OF TEMPERATURE COEFFICIENT



CLASS II DIELECTRICS

Class II dielectrics comprise the ferroelectric formulations described in Section H. These materials offer much higher dielectric constants than Class I dielectrics, but with less stable properties with temperature, voltage, frequency and time. The diverse range of properties of the ferroelectric ceramics requires a subclassification into two categories, defined by the temperature characteristics:

"Stable Mid-K" Class II, which display a maximum temperature coefficient of ±15% from 25˚C reference over the temperature range of -55˚C to 125˚C. These materials typically have dielectric constants in the range of 600 to 4000, and meet EIA X7R characteristics.

"High K" Class II dielectrics, with temperature coefficients exceeding the X7R requirements. High K formulations display dielectric constants from 4000 to 18,000, with very steep temperature coefficients, due to the fact that the Curie Point is shifted towards room temperature for maximization of the dielectric constant.

Table J-2 shows the EIA 198 descriptions for these dielectrics. The most common Mid-K characteristic used in chip capacitor manufacture is the X7R designation (±15% maximum ΔC from -55˚C to 125˚C). In the High-K category, the Z5U characteristic (+22% to -56% maximum ΔC from +10˚C to +85˚C) and Y5V (+22% to - 82% maximum ΔC from -30˚C to +85˚C) are common.

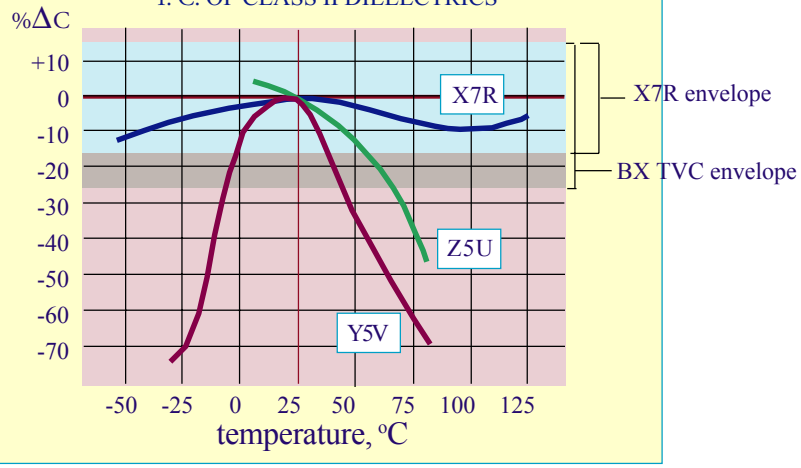
The military specification for ceramic chip capacitors (MIL-C-55681) also defines the Mid-K stable

TABLE J - 2
EIA DESIGNATIONS FOR CLASS II DIELECTRICS

(a)	(b)	(c)	(d)	(e)	(f)
low temperature requirement	letter code for (a)	high temp. requirement	numerical codes for column (c)	Max. (+/-)%ΔC over temp.	letter code for column (e)
+10	Z	+45	2	1.0	A
-30	Y	+65	4	1.5	B
-55	X	+85	5	2.2	C
		+105	6	3.3	D
		+125	7	4.7	E
				7.5	F
				10.0	P
				15.0	R
				22.0	S
				+22-33	T
				+22-56	U
				+22-82	V

dielectric and is designated as "BX" characteristic. The BX specification has voltage temperature limits in addition to the standard temperature limits discussed previously. BX dielectric is limited to a ±15% maximum capacitance change from -55˚C to 125˚C, and to a +15% -25% maximum change with working voltage applied. In effect, the BX characteristic is similar to the X7R designation, with the added condition that the voltage coefficient and temperature coefficient combined do not exceed +15% -25%ΔC. Typical Class II T.C. curves are shown in Figure J-3.

FIGURE J - 3
T. C. OF CLASS II DIELECTRICS



K. TEST PARAMETERS AND ELECTRICAL PROPERTIES

Electrical behavior of ceramic chip capacitors is strongly dependent on test conditions, notably temperature, voltage and frequency, for reasons explained in Sections F through I . This dependence on test parameters is more notable with Class II ferroelectric dielectrics, and negligible or more easily predictable with Class I formulations. For this reason, certain standards of measurement have been established in the industry, with the appropriate limits of performance for any given electrical property and dielectric characteristic.

TEMPERATURE DEPENDANCE

Temperature Coefficient (Capacitance-Temperature Dependance): The variance of capacitance with temperature is used to classify dielectric formulations, as described in Section J. In general, it is found that materials with higher dielectric constants at 25˚C display greater change with temperature, on the hot or cold side of reference, as the higher K materials are based on formulations which shift the sharp Curie peak to room temperature. Lower K dielectrics, which are formulated to suppress and broaden the Curie peak over temperature, display more stability, as intended. This effect is clearly evident in the curves of Figure J-3 for X7R and High-K dielectrics.

The temperature coefficient (T.C.) is expressed in ppm/˚C for Class I type ceramics, and as %ΔC for Class II. Measurements are obtained by maintaining chip capacitor samples under controlled temperature conditions in a temperature or "T.C." chamber, while accurate readings of capacitance are made at various temperatures, usually -55˚C , 25˚C and 125˚C. Accuracy of fixtures and test equipment is obviously important, especially when measuring lower capacitance values where small changes in ppm/˚C may provide only a fraction of a picofarad in capacitance change from the reference value. Care must also be exercised when measuring higher value Class II dielectrics, due to the de-aging property of these materials. The de-aging of samples at the hot stage of the measurements may result in erroneous T.C. calculations; it should be a practice to de-age these capacitors for a minimum of one hour before T.C. measurements are made.

The temperature coefficient for Class I dielectrics is calculated in ppm/˚C for any given temperature range, using the following expression:

$$T.C.\ (ppm/^{\circ}C) = [(C_2 - C_1) / C_1(T_2 - T_1)]10^6$$

where: C_1 = capacitance @ T_1
C_2 = capacitance @ T_2
and $T_2 > T_1$

Examples: Capacitance measurements at temperature are as follows:

-55˚C, 1997 pF
25˚C, 2000 pF
125˚C, 2004 pF

Computation of the T.C. slope for the -55˚C to 25˚C range:

$$T.C. = [(2000-1997)\ 10^6] / 1997[25-(-55)] = 18.7\ ppm/^{\circ}C$$

Computation of the T.C. slope for the 25˚C to 125˚C range:

$$T.C. = [(2004-2000)\ 10^6] / 2000(125-25) = 20.0\ ppm/^{\circ}C$$

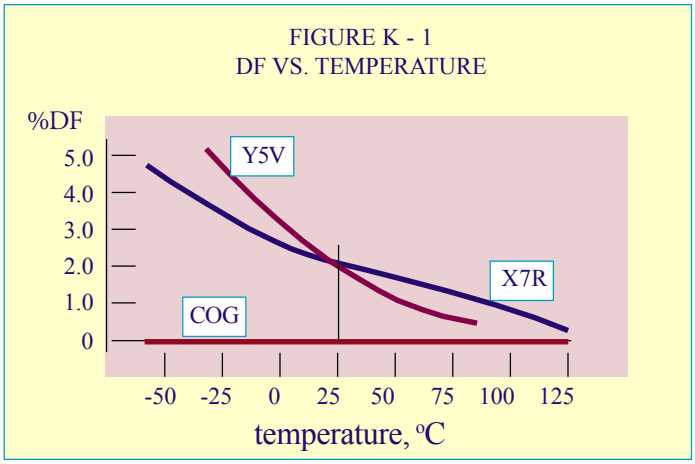
The temperature coefficient for Class II dielectrics is reported as the percent change from the room temperature measurement, as the variations observed are several orders of magnitude greater than those for the linear dielectrics.

The acceptable limits for any given dielectric characteristic are specified in the EIA 198 specification, as shown in Tables J-1 and J-2.

Dielectric Loss and Temperature: Class I dielectrics display only negligible change in dissipation factor with temperature over the standard -55˚C to 125˚C temperature range. Industry standards require that at 25˚C the DF is not to exceed .001 (0.1%) for standard linear dielectrics (COG-NPO) and not to exceed .002 (0.2%) for the extended T.C. series of dielectrics.

Class II dielectrics show a general decrease of DF with temperature, notably at or near the Curie Point of the material. Above the Curie Point, the energy consuming ferroelectric domains no longer operate and internal losses are minimized. At temperatures below the Curie Point, the domain relaxation processes for any given Vac signal are activated, and energy loss is reflected in an increase in the dissipation factor. The complexity of the ceramic microstructure and the resultant multiple Curie Points of the aggregate polycrystalline components in any given formulation do not permit a clear prediction of DF behavior with temperature, other than the fact that DF is inversely proportional to temperature. Industry standards for Mid-K dielectrics, such as X7R, require that at 25˚C the DF not exceed .025 (2.5%). High-K dielectrics, such as Z5U and Y5V, are often specified with a maximum DF of .030 (3.0%) at 25˚C. Typical DF curves with temperature are shown in Figure K-1 for several dielectrics.

FIGURE K - 1
DF VS. TEMPERATURE



Insulation Resistance and Temperature: The properties which give rise to the insulation resistance of dielectrics were outlined in Section G-1. As described in that portion of the text, the mechanisms of conduction are temperature dependent, and leakage of current increases with temperature, as added thermal energy increases the diffusion of charge carriers. It is found that in general the IR of most dielectrics at 125°C decreases by a factor of one to two orders of magnitude from the 25°C measurement. Industry standards require that the IR readings at 125°C exceed 100 ohm-Farad, (10% of the values shown in Table G-1).

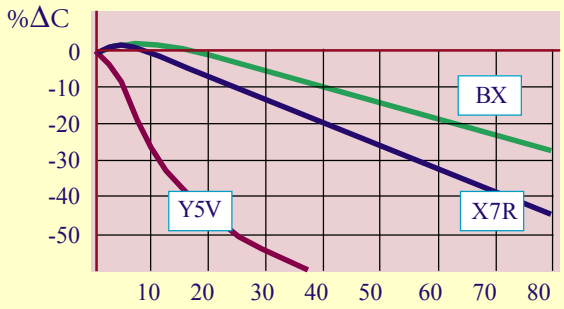
Dielectric Strength and Temperature: The dielectric strength of insulators is inversely proportional to temperature, as heat lowers the intrinsic resistivity of the material as discussed previously. As a general rule, a properly designed capacitor of sound construction should withstand the normal 25°C dielectric withstanding "flash" voltage at 125°C.

VOLTAGE (VDC) DEPENDANCE

Vdc Coefficient: Ferroelectric Class II formulations are sensitive to dc voltage. In all cases an eventual decrease in dielectric constant occurs with dc bias, which is more severe with dielectrics of higher dielectric constant. This behavior is attributed to a constraint of the dc voltage on the response of the polarizing mechanisms which give rise to the dielectric constant of the material.

The curves of Figure K-2 are data for various formulations. The curves show the expected capacitance change with increased volts/mil dc bias. As is evident from these data, consideration of the effect of dc bias requires knowledge of the construction of the capacitor, as the thickness of the individual dielectric layers will determine the volts/mil loading of the device during operation. In effect capacitors of identical capacitance value and voltage rating may behave quite differently depending upon internal construction.

FIGURE K - 2
VOLTAGE COEFFICIENTS



Consider the following examples:

a. Capacitor of 0.1 mfd, constructed of 20 layers, 1.0 mil thick, X7R dielectric, rated at 50 volts: The predicted capacitance change, based on the data of Figure K-2, is -25%, as the dielectric is stressed at 50 volts/mil when operating at 50 Vdc.

b. Capacitor of 0.1 mfd, built with the same dielectric, but constructed with 30 layers 1.5 mils thick. At 50 Vdc. operation, however, the dielectric layers experience only 33 volts/mil, and the predicted capacitance change is therefore reduced to -15%.

c. Capacitor of 0.1 mfd, built with 40 layers of 2.0 mil dielectric will experience only 25 volts/mil at 50 Vdc, and the predicted capacitance change is further reduced to -10%. The effect is of considerable importance in the design of capacitors intended to meet characteristics which require that the combined temperature and voltage coefficients (TVC) not exceed a certain ΔC over the operating temperature range, at working voltage. Assuming that a dielectric is available with T.C. characteristics well within the ±15% max ΔC, the manufacturer need only be concerned with the negative contribution of the voltage coefficient. For the examples stated above, and assuming that the T.C. of the dielectric utilized varies typically ±7% maximum, the maximum TVC for the three examples are as follows:

	T.C.	VC	Max. TVC	Characteristic
a.	+7%-7%	-25%	(+7%-32%)	X7R only
b.	+7%-7%	-15%	(+7%-22%)	X7R and BX (marginal)
c.	+7%-7%	-10%	(+7%-17%)	X7R and BX

Voltage Conditioning - Aging Effects: Class II dielectrics experience an accelerated aging effect when stressed by dc voltage, as briefly described in Section G-3. This effect is evident even at room temperature, and is more dominant at higher voltage and with dielectrics with elevated dielectric constant. In the manufacture of close tolerance (±5%) Mid-K dielectrics, or high voltage units, the product is usually reheated after IR or dielectric withstanding voltage testing, to maintain capacitance tolerance and establish a fresh aging cycle. X7R units may derate as much as 3% in capacitance after dc withstanding voltage testing at 300 volts/mil.

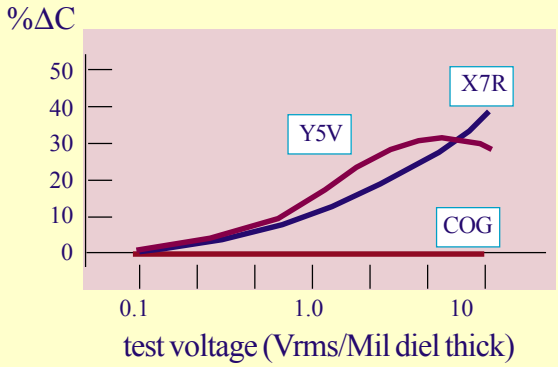
DF and dc Voltage: Class II dielectrics experience a decrease in dielectric loss with increasing voltage. The DF may be reduced by a factor of 75% at 100 volts/mil bias for X7R dielectric.

AC VOLTAGE DEPENDANCE

AC Voltage Coefficient: Class II dielectrics are fairly sensitive to test voltage, which can create significant changes in the measured dielectric constant, as illustrated in Figure K-3. The response to AC voltage always shows an increase in dielectric constant with the AC signal, with the higher K dielectrics responding more readily, until some threshold voltage value is reached where the effect reverses. Class I dielectrics, operating in the paraelectric state, display negligible or only limited response to the AC bias.

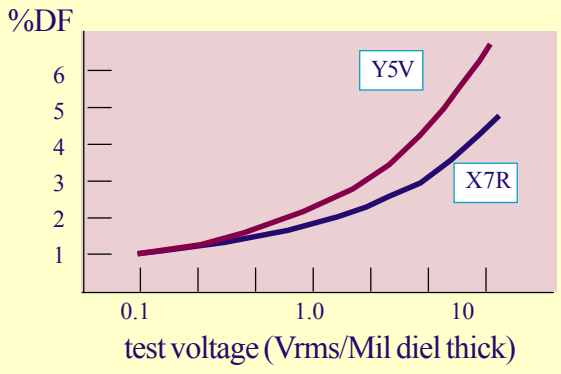
Industry standards specify a test voltage of 1.0 +/- 0.2 Vrms for all dielectrics with the exception of some High-K less stable Class II bodies which are specified by manufacturers at 0.1 or 0.5 Vrms, typically. Application of these materials at other voltages therefore presents correlation problems, even at low voltage stress (under 5 Vrms/mil) as evident from the data of Figure K-3. As occurs with the interpretation of dc voltage coefficient, the situation is further complicated by the added variable of capacitor design, i.e. dielectric thickness of the individual layers.

FIGURE K -3
AC VOLTAGE COEFFICIENT



Dielectric Loss and AC Voltage: The increase of dielectric constant with AC test voltage is accompanied by a marked increase in the dissipation factor, as illustrated in Figure K-4. The multilayer construction of chip capacitors, with thin dielectric layers, precludes application in circuitry with large AC voltage and high current, as dielectric losses become quite significant between 5 and 20 Vrms/mil stress.

FIGURE K -4
AC BIAS EFFECT ON DIELECTRIC LOSS



FREQUENCY DEPENDANCE

The close interrelationship of frequency and dielectric polarization and dielectric loss was described in some detail in Sections F-2 and F-4. Increased frequency of an applied field results in a decrease of the measured capacitance value. This dependence is due to the inability of some of the polarizing processes to respond to the ever faster polarity reversals of the field, such that the net contribution of polarization to the dielectric constant of the material is reduced, and the dielectric loss is increased. These effects are common to all the dielectric groups, but are more predominant in the ferroelectric formulations which display large ionic polarization. Typical curves for capacitance and dissipation factor versus frequency are illustrated in Figures K-5 and K-6.

AGING -TIME DEPENDANCE

The phenomenon of ferroelectric dielectric aging is described in Section G-3. Restraints on the % per decade hour aging rates are usually specified by users of chip capacitors. X7R is expected to age less than 2.5%/decade hour, and most dielectrics within this characteristic typically have aging rates from 0.8% to 2.0% per decade hour. The High-K aging specification is more liberal by necessity; an aging rate of 5% per decade hour is considered normal.

Many of the Class II dielectrics may also display aging of the dissipation factor, an effect more predominant with High-K formulations.

FIGURE K -5
CAPACITANCE VS. FREQUENCY

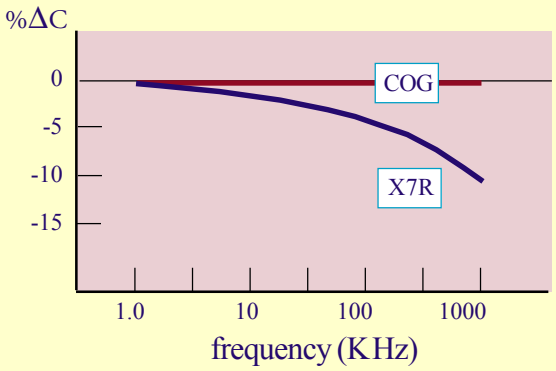
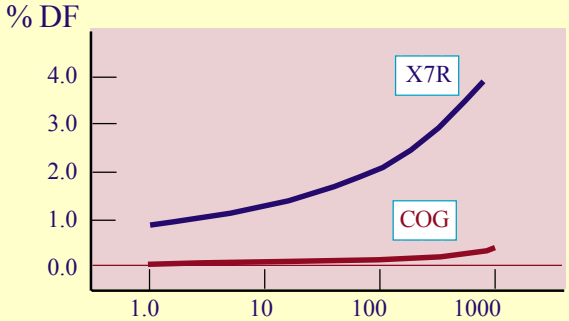


FIGURE K -6
DF VS. FREQUENCY



L. INDUSTRY TEST STANDARDS

Chip capacitor test parameters, performance specifications and quality conformance requirements are outlined in the EIA 198 and MIL-C-55681 specifications. A summary of electrical specifications for popular Class I and Class II dielectrics is presented in Table L-1. Relevant EIA and MIL test methods and quality conformance requirements (most commonly applicable to MLC capacitors) are given in Table L-2.

TABLE L-1
ELECTRICAL SPECIFICATIONS FOR CLASS I AND CLASS II
DIELECTRICS - EIA 198 AND MIL-C-55681

	COG or NPO EIA 198, MIL-C-55681	BX MIL-C-55681	X7R EIA 198	Z5U EIA 198	Y5V EIA 198
Oper. Temp.Range	-55°C to 125°C	-55°C to 125°C	-55°C to 125°C	10°C to 85°C	-30°C to 85°C
Temp. Coefficient %ΔC Max., 0 Bias	0 +/- 30 ppm/°C	+/- 15%	+/- 15%	+22% -56%	+22% -82%
Temp-Volt Coeff. %ΔC Max., @ Vdc	0 +/- 30 ppm/°C	+15% -25%	N/A	N/A	N/A
Dissipation Factor, @ 25°C	0.10% Max.	2.5% Max.	2.5% Max.	3.0% Max.	5.0% Max.
Insulation R @ Vdc, 25°C	>100GΩ or >1000ΩF	>100GΩ or >1000ΩF	>100GΩ or >1000ΩF	>10GΩ or >100ΩF	>10GΩ or >100ΩF
Insulation R @ Vdc, 125°C	>10GΩ or >100ΩF	>10GΩ or >100ΩF	>10GΩ or >100ΩF	N/A	N/A
Dielectric Test Voltage, 25°C	250% WVdc	250% WVdc	250% WVdc	250% WVdc	250% WVdc
Aging Rate, Max %ΔC/decade	0%	-2.0%	-2.5%	-3.0%	-5.0%
Test Frequency, 25°C	<100 pF, !.0MHz >100pF, 1.0 KHz	1.0 KHz	1.0 KHz	1.0 KHz	1.0 KHz
Test Voltage, 25°C	1.0 +/- 0.2 Vrms	1.0 +/- 0.2 Vrms	1.0 +/- 0.2 Vrms	0.5 +/- 0.2 Vrms	0.5 +/- 0.2 Vrms

Note: The dielectric withstanding test voltage shown in the table applies to voltage ratings for 200V or less. Typically, the following test voltages apply for varied ratings:

16V to 200V:	250% WVdc
>200V <500V:	150% WVdc, or 500V: whichever is greater
<500V:	120% WVdc, or 750V: whichever is greater

TABLE L-2
GENERAL TESTING AND QUALITY CONFORMANCE
SPECIFICATIONS FOR CHIP CAPACITORS

Specification	Test Category	MIL Method Number	EIA-198-1-E Method	Test Description
EIA-198-1-E MIL-C-55681: MIL-STD-202F (MIL-STD-883E)	Environmental	103B 104A (1002) 106F (1004.7) 107G (1011.9) 108A (1010.7)	205 203 204 202 201	Humidity Immersion Moisture Resistance Thermal Shock Life (@ elevated Temp.) Temperature Cycling
EIA-198-1-E MIL-C-55681: MIL-STD-202F (MIL-STD-883E)	Physical	204D 208H (2003.7) 210E 211A 212A 213B (2002.3) 215J (2001.2)	304 301 302 303 305 210 306 (EIA-469-C)	Vibration Solderability Resistance to Solder Heat Terminal Strength Acceleration Shock Resistance to Solvents Constant Acceleration Destructive Physical Analysis
EIA-198-1-E MIL-C-55681: MIL-STD-202F (MIL-STD-883E)	Electrical	301 302 (1003) 305 306	103 104 101 102 105	Dielectric Withstanding Voltage Insulation Resistance Capacitance and DF Quality Factor Voltage-Temp. Cap Coefficient
MIL-PRF-49467A		Appendix B		Partial Discharge (High Voltage)

M. HIGH RELIABILITY TESTING

BURN IN

Dielectric formulations and chip capacitors are often tested for reliability under voltage and temperature for specified time periods, a process referred to as “burn in” or “voltage conditioning”. Specifications applicable to burn in of MLC capacitors are MIL-C-55681, MIL-C-123 and MIL-C-49467. Burn in may also be performed to particular customer specifications. The test voltage is usually twice the working voltage rating of the device, at 85°C or 125°C for a duration of 96 hours, 100, or 168 hours test time, typically.

Burn in is accomplished by loading of units in a fixture, usually a PC board which contacts to a power supply with access to the rear wall of a standard oven. Units are monitored for current leakage under voltage and temperature stress either individually or in tandem, with measurement of leakage from a group of a hundred units, typically. Tandem testing is more rapid and used to mass produce burned in product. Sophisticated equipment is used with automatic data monitoring to record the location and time of test cycle failures.

Chip capacitors destined for high reliability testing are often designed with an added margin of safety, namely maximization of the dielectric thickness, and tested extensively for electrical properties prior to burn in (capacitance, DF and insulation resistance). These data are compared to post life test data for evaluation of the reliability of the components.

FAILURE MODES

Capacitors which fail burn in usually lose resistivity at the elevated temperature and voltage, either catastrophically, or gradually with time, resulting in IR rejects. The failure rate is usually inversely proportional with time, i.e. more failures are observed earlier in the test cycle.

Excellent electrical properties at 25°C may not guarantee good performance during life test (hence the purpose of the test), for several reasons:

Poor dielectric properties: Ceramic dielectrics with elevated insulation resistance at room temperature may nevertheless experience excessive loss of resistivity at 125°C due to improper formulation, whereby charge carriers become mobile and develop a leakage current, decreasing the insulation resistance below specifications.

Poor microstructure: Voids, cracks or delaminations within the chip structure undermine the intrinsic resistivity of the material, providing leakage paths conducive to failure. This does not imply, however, that units which survive life testing are always free of microstructural defects. Experience has shown that despite rigorous testing, units with delaminations may still perform adequately, while failures may be observed in units with apparent “excellent” microstructure. This is due to the fact that delaminations may often affect only the plane of the electrodes, without serious deterioration of the dielectric between electrodes of opposite polarity. Cracks, voids or impurities which straddle the electrode array are more conducive to eventual degradation under voltage and temperature. The latter defect may be microscopic in magnitude, and not easily observed or located within the chip microstructure, which may otherwise appear quite normal.

A second failure mode independent of the above, is degradation of the capacitance value and/or dissipation factor of the chip capacitor, i.e. post burn in data does not correlate well to the original

electrical test data.

Class I dielectrics, which are non-ferroelectric, do not exhibit capacitance aging with time, temperature or voltage. Any burn in induced capacitance change in Class I chips is associated with mechanical failure, such as cracking which isolates electrode layers. Class II dielectrics, however, may display capacitance and dissipation factor variations after bum in without mechanical failure, as these dielectrics are time, temperature and voltage dependent. Most notably, the accelerated aging of the dielectric constant under burn in conditions must be considered for proper interpretation of results; units under test may be exposed to three very different aging scenarios, depending on the method used to terminate the life test. The following three conditions assume that pre-burn in data was performed on de-aged units:

a. The voltage is removed while the units are at temperature, and temperature is maintained with no bias for a minimum of one hour. Under this condition, total de-aging of capacitors occurs, and units will display minimal (positive or negative) capacitance change with respect to the original pre-burn in values.

b. Capacitors remain under dc bias while the oven is permitted to cool to room temperature. This in effect is a voltage conditioning process and the units will therefore age with respect to the original test data, e.g. -7.0% ΔC.

c. The voltage is removed at the burn in temperature and the units subsequently taken from the oven and allowed to air cool to room temperature. In this case, the units do not fully age during the cooling cycle, as in example (b), nor do they totally de-age as in (a) above. The components thus experience a partial aging only, e.g. -3.5% ΔC.

The $\%\Delta C$ values given as examples for the post burn in data above are typical of some Mid-K dielectrics. High-K less stable dielectrics may experience more radical capacitance changes, as these materials have an aging rate of 5% per decade hour typically, three times the average rate of X7R formulations. These considerations clearly indicate that procedure (a) only should be followed for termination of the life test for proper evaluation of performance of Class II dielectrics.

In addition to burn in, high reliability often involves other performance tests, as outlined in Table L-2, per MIL-C-55681 or to customer specifications. The most common of these additional tests are dielectric withstanding voltage and insulation resistance at elevated temperature, voltage-temperature limits, thermal shock, solderability and solder leach resistance of the chip capacitor termination. In addition, strict visual and mechanical examination of the product may be required, including Destructive Physical Analysis (DPA). The various group categories of high reliability testing applicable to MIL specifications are outlined in Table M-1. Any or all of the Group tests may be specified by customers requiring high reliability product.

TABLE M-1
HIGH RELIABILITY TEST PROCEDURES

Specification	MIL-C-55681	MIL-C-123B
GROUP A	Voltage Conditioning IR @ Elevated Temperature Visual & Mechanical Inspection ESR, when Specified Solderability	Thermal Shock Voltage Conditioning Visual & Mechanical Inspection, Destructive Physical Analysis
Specification	MIL-PRF-49467A (High Voltage)	MIL-PRF-39014F (Leaded Devices)
GROUP A	Thermal Shock Voltage Conditioning Partial Discharge Radiographic Inspection Mechanical Examination Visual Examination Solderability	Thermal Shock Voltage Conditioning Radiographic Inspection Mechanical Examination Visual Examination Solderability
GROUP B GROUP C	Environmental and Life Tests performed for qualification, or to attain Established Reliability, applicable to any specification, if required.	

N. VISUAL STANDARDS FOR CHIP CAPACITORS

EXTERNAL VISUAL STANDARDS

MLC capacitors must possess fine workmanship and physical integrity. Visual inspection of chip capacitors involves observation of the product under 20X magnification, for major and minor defects in workmanship in the capacitor body and end metallization. Visual standards are detailed in MIL-C-123B, Appendix C, and apply to the chip body, metal terminations, chip edges, surfaces and marking, if applicable. Typically, manufacturers inspect only sample quantities, in accordance with MIL STD 105, Level II, 0.65. Acceptance or rejection of standard production lots is based on various defective (AQL level or ppm level) criteria. The nature of the defects is listed in Table N-1 and depicted in Figure N-1.

TABLE N-1
TYPICAL CRITERIA FOR VISUAL DEFECTS

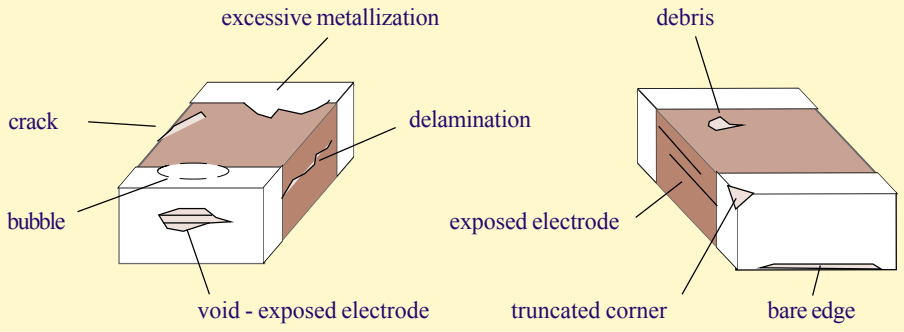
Major Defects:

1. Cracks, blisters, raised surfaces or delaminations in the capacitor body.
2. Chips or voids in the capacitor body which exceed .003" (.08mm), or which expose internal electrodes.
3. Foreign debris bonded to the chip surface, which exceeds .005" (.13mm)
4. Miscutsof the capacitor edge which penetrate the surface by more than .005"(.13mm), or expose internal electrodes. Flared edges.
5. Termination defects:
   - Voids in the termination which expose electrodes.
   - Voids in the termination exceeding .005" (.13mm).
   - Exposed metallized edges which exceed 10% of edge dimension.
   - Bare corners on metallized ends.

Minor Defects:

1. Minor irregular cuts of sides or corners
2. Foreign debris on capacitor surface not exceeding .005" (.13mm).
3. Termination Defects:
   - Voids in metallization less than .005" (.13mm).
   - Exposed metallized edges which do not exceed 10% of edge dimension.
   - Poor marking (if applicable)

FIGURE N-1
VISUAL DEFECTS



INTERNAL MICROSTRUCTURE STANDARDS

In addition to the external visual characteristics, quality standards for internal microstructure of the chip capacitor are also applicable, as viewed on polished cross sections of capacitor samples. Units are sectioned along the long and short dimension of the capacitor to provide two edge views of the internal electrodes and terminals.

Although any degree of internal defect is considered undesirable, the fact remains that these types of defects can occur occasionally in different degrees of severity. Typically, delaminations, internal voids, cracks and other irregularities are classified as to their severity, and are considered to constitute defects if they exceed the following, as based on EIA 469. (Refer also to Figure N-2.).

Delaminations

A delamination is a separation of the structural layers of the capacitor, in the form of a planar cavity, between the electrode and ceramic, or within the dielectric itself. Any delamination which can be considered to be detrimental to the electrical and mechanical integrity of the capacitor is classified as a defect, and generally involves the following:

Any delamination in the active (electrode overlap) area, longer than 20% of the electrode length, or exceeding .010" (.254 mm), whichever is greater.

Any delamination greater than .005" (.127 mm), located within the electrode overlap area, and associated with displacement of adjacent electrodes and reduction of these dielectric layers by more than 50% of their thickness.

A delamination which exceeds 50% of the margin between the termination and electrodes of opposite polarity.

Two or more delaminations exceeding .010" which overlap each other in the active electrode area, in adjacent layers.

Voids

Any void which can be considered detrimental to the electrical and physical integrity of the capacitor is classified as a defect, and generally involves the following:

Any void between electrodes of opposite polarity, which reduces the dielectric thickness by more than 50%.

Any void in the cover plate of the capacitor which reduces the cover thickness to less than .003" (.076 mm), or less than the active dielectric thickness.

A void or bubble in the termination ,not contacting the dielectric surface, which exceeds 30% of the chip end dimension.

A void or bubble in the termination, contacting the dielectric, which exceeds .020" (.508 mm).

Cracks

Any crack which can be considered detrimental to the electrical and physical integrity of the capacitor is classified as a defect, and generally involves the following:

Any crack connecting any two electrodes.

Any crack connecting an electrode to any exterior surface of the chip, or to a termination. Cracks extending from the termination metal band into the interior of the chip (termination stress crack).

Non-Uniformities

Irregularities in the construction of the chip capacitor do not necessarily affect the mechanical or electrical integrity of the device, but may be of concern in high reliability applications. The following is a compilation of structural irregularities according to the EIA 469:

A side or end margin of dimension less than .003" (.076 mm) between 90% or more of the electrodes and the exterior dielectric surface.

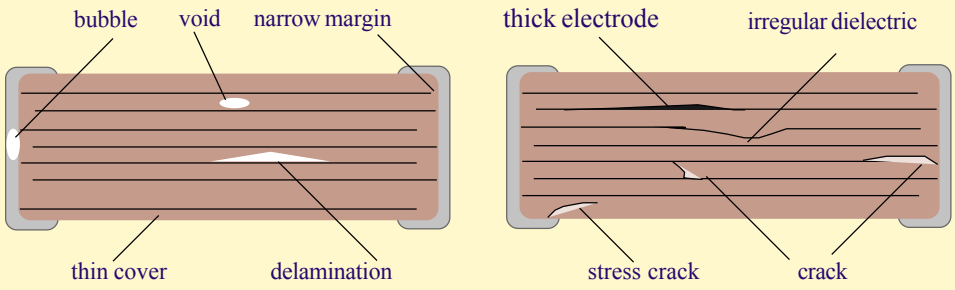
Ceramic cover plate thickness which is less than the dielectric thickness between adjacent electrodes.

Variations in the active dielectric layers which result in areas with less than 50% of the nominal dielectric thickness.

Thick electrode depositions, exceeding 2.5 times the average electrode thickness, and extending over 50% of the electrode length.

Thick electrode deposition, extending over .005" (.127 mm), which also reduces the adjacent dielectric layer thickness by more than 30%.

FIGURE N-2
MICROSTRUCTURE DEFECTS



Sample Preparation Defects

A variety of imperfections observed on sectioned specimens can arise due to the method of sample preparation, and must be so identified, so as to preclude erroneous interpretation of results. Subtle observations and precautions can be followed to positively segregate preparation problems from actual defects. First, it is essential that the specimen be observed, prior to mounting in a section, to determine if any obvious mechanical flaws are present. Usually this is accompanied by inspection of basic electrical properties. Secondly, units must be rigidly encapsulated, with non-shrinking (and hence stress-free) resin, and be ground and polished with fine grit abrasives under controlled pressure, to avoid cracking. Sections must be polished to remove all vestiges of the rough cuts used to reduce the specimen, and be cleaned thoroughly before observation. This procedure will minimize the occurrence of most sectioning induced defects (depicted in Figure N-4).

The following criteria are used to attribute defects to sectioning methods:

Void defects form linear patterns, i.e. they are induced by grit pulling material out of the ceramic during grinding, hence more polishing is required. Note that voids forming a line parallel to the layered structure of the device, a so called “knit line”, may not fall into this category.

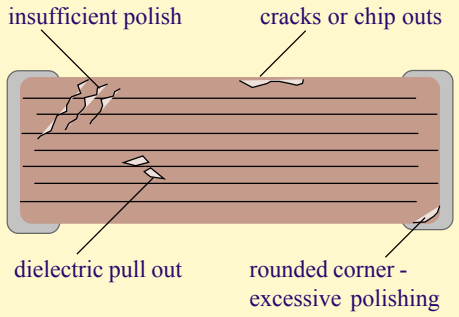
Large voids are present, with virtually no distortion of the electrode pattern or of adjacent dielectric layers. The correctness of the structure around these voids is indicative as to their absence in the original unsectioned unit; thermal processing would otherwise result in collapse of electrode and/ or distortion of layers around these voids. Such defects are caused by excessive pullout during grinding, particularly in the area between electrode layers, where there is minimal dielectric layer to layer bonding.

Units exhibit cover sheet cracks, and/or separation of the ceramic cover sheet from the electrode array, yet were not evident on usual examination of the device prior to sectioning. These defects arise due to insufficient support in the encapsulant, and/or excessive grinding methods. Such cracks may also appear parallel to the end terminations, as the termination to ceramic interface is mechanically weaker; measurements of capacitance, DF and insulation resistance, as well as termination pull strength can be used to confirm the absence of this defect in unsectioned product.

Excessive polishing will round corners and edges of the section, resulting in depth of field distortions on observation, as well as difficulty with illumination. 'Defects' which appear under these conditions may be non existent and should be disregarded.

Evaluation of visual and microstructure quality of chip capacitors is very subjective, and difficulties arise in correlating opinions between observers, especially when considering the minor category of defects described above. In addition, dissimilar images can occur when viewing product under differing light sources on a microscope. Fluorescent lighting has been found to be superior over incandescent light in highlighting defects.

FIGURE N-4
SAMPLE PREPARATION DEFECTS



The acceptance or rejection of capacitors with any visual or microstructure defects is usually specified or determined by the chip user, based on the application of the product. High reliability or high voltage units must meet the stringiest standards.

O. CHIP USER GUIDELINES

Multilayer ceramic capacitors are sold as chip (leadless) components, or as encapsulated leaded devices. Traditionally, the chip version has been used in densely packed hybrid and delay line circuits, while the leaded capacitor has dominated the high volume printed circuit board market, which is tooled for automatic insertion of axial or radial lead devices of all types. Leaded components, packaged in tape and reel format, per EIA Standard RS 296, are assembled or "stuffed" into plated through holes on P.C. boards by high speed in line assembly machines.

The need for higher packaging densities of components on P.C. boards has led to the development by the Japanese of " surface mount technology" which involves high speed automatic placement of leadless components. As with leaded devices, this method requires the chip components to be packaged in tape and reel format, to serve as feeder spool to placement machines, or handled at high speed by chip feeders. Chip components are typically placed in 8 mm wide perforated and sealed cardboard tape, or in embossed plastic carrier (EIA Standard RS 481). The placement machine removes the chip from the carrier and "tacks" the devices to a hybrid substrate or P.C. board, with non conductive epoxy. Subsequent soldering and attachment of the components onto the circuit is accomplished with conventional solder wave processing.

The advent of surface mount technology, and high speed placement of chip capacitors in bulk form, has greatly increased the use of chip capacitors in all circuitry. Variables affecting attachment of chips to substrates are therefore of increasing importance, regardless of the method used for placement of the devices. The inherent mismatch of thermal and physical properties of components to substrates and solders is somewhat buffered with the use of leaded devices, which are isolated by virtue of the leads themselves. In contrast, this mismatch is intensified by the use of chip components directly bonded to the substrate material.

CHIP CAPACITOR ATTACHMENT METHODS

Chip bonding to substrates can be categorized into two general classes; methods involving solder, which are prevalent, such as reflow soldering, and those involving other bonds, such as epoxies, and wire bonds (thermal-compression and ultrasonic bonding).

Soldering

Solder attachment can be accomplished in a variety of ways: hand soldering of chips to substrate pads; reflow of pre-tinned capacitors on pre-tinned substrate pads; reflow of capacitors on substrate pads covered with a solder preform or with screened on solder paste, or wave soldering of chips and substrate, with chips held in position with non conductive epoxy. The latter provides the advantage

that units may be attached to both sides of the substrate, thus increasing packing densities.

A common method used in the surface mount industry is the solder paste reflow technique, and involves the following basic steps:

The surfaces to be joined are to be prepared by cleaning and pre-fluxing. Capacitors and substrate are cleaned with isopropanol or other mild solvent which does not leave residues detrimental to the circuit. Chips with excessively tarnished end metallizations, due to prolonged storage, may cause soldering difficulties. A new metal surface can be attained by firing of the chips to approximately 700°C.

Chip and substrate contact areas are pre-fluxed with a mild organic flux, which is easily removed with an azeotrope solvent after soldering. Examples of such fluxes are Kester 1544 and Kester 1545.

The substrate is pre-tinned with solder, using screened on solder paste, or by dipping of the substrate into molten solder, or with the use of solder preforms. The volume of solder required is one that results in a well formed solder fillet. Inadequate or excessive solder may result in undesirable residual stresses on the chip component.

The capacitor-substrate assembly is heated to the solder flow point temperature, allowing sufficient time for wetting of the solder to the metallized surfaces to occur, to form a well rounded fillet. Excessive time at the solder reflow temperature is undesirable due to the formation of intermetallic compounds. A controlled temperature profile, as obtained with a reflow furnace, is required to preclude thermal shock hazards.

The assembled substrate is cleaned with a mild solvent, usually by ultrasonic means, to remove flux residues from under and around the bonded chip. Total cleaning is possible as the component is somewhat elevated above the substrate surface, by virtue of the combined thickness of the conductor pad, the chip end metallization and the surface tension action of the solder in the molten state.

The advent of high component density circuits, which utilize surface mount technology, has resulted in the need for more thermal efficient and reliable soldering methods. Surface mount components are attached to the substrate by pick and place machines, and held in place by epoxy or solder paste for subsequent processing, which may involve any of the following:

Infrared (IR) solder reflow: (briefly described above): The advantage of this method is that precise temperature profiles are possible, and hence control of the many parameters of the circuit assembly can be maintained, including volatilization of solvents, activation of fluxes,

solder reflow and wetting time, and uniform and gradual cooling.

IR heat transfer is by direct radiation, and different, specific profiles need to be established for variations in board type and configuration. In general, however, IR profiles should include several minutes of time at temperatures below 100°C where solvents volatilize, to cure the thick film solder paste, and thus minimize the occurrence of blow holes, or solder splash, which result in solder balls. A preheat cycle of one to three minutes should follow, to gradually increase the temperature from 100°C to a temperature just below the solder melting point, before a rapid, less than 10 second 30°C spike, to attain solder wetting, and the formation of clean, well formed fillets. Several minutes of gradual cooling are required to terminate the cycle without inducing undesirable thermal stresses (see section 0-2.)

Vapor Phase Reflow: This method is based on rapid and thermally efficient transfer of heat from hot vapors to the hybrid assembly. Boards are located above a boiling fluid which creates a vapor phase of specific peak temperature; fluids are selected to suit the reflow point of solder types. The advantage of this system is that total immersion of the circuit in the hot vapor provides a more uniform heat transfer. The process is therefore less selective as to the characteristics of the board, but also more stressful, as the heat transfer can be very rapid. Problems may arise unless a preheat cycle is incorporated to prevent sudden outgassing of paste constituents and thermal shocking of components, and profiles are thus restricted by the circuit assembly, as with other reflow methods.

Solder Wave: This technique is in contrast to the above in that soldering is accomplished by direct contact of the hybrid assembly to molten solder. The circuit is transported through programmed flux, preheat, soldering and cooling cycles. Total immersion in flux and molten solder is attained by pumping of these through a fixture to create a constantly flowing crest or “wave” of sufficient height to cover the circuit in its entirety as it is conveyed through. Some machines utilize dual solder waves to maximize solder wetting,

The preheat cycle is included to prevent thermal shocking of components; the preheat dwell time and temperature are adjusted to attain rapid yet controlled heating of the board to approach the peak temperature of the solder wave within 50°C, in 20 to 60 seconds. Similarly, a controlled cooling cycle of several minutes follows to minimize thermal stresses within the components and/or bonds, which arise due to the thermal properties of chip capacitors, as described in section 0-2.

Regardless of which of the above methods is utilized for chip attachment, it should be noted that as with all situations of heat transfer, whether by radiation, convection or conduction, other factors over which there is little degree of freedom play a limiting role. These factors include the physical properties of the material, such as its mass, heat capacity, thermal coefficient and diffusivity, en-

thalpy, and other extraneous factors, such as velocity of gases, reflectivity to radiation, and temperature differences within the system.

The objective of any solder attachment system is the same: to attain clean and smooth solder joints, with no bridging or open areas, i.e. wetting quality and solder quantity should be optimized, and without physical defects, such as cracks, cold joints, pinholes, etc. Not all these parameters are solder processing dependent, as certain defects can be attributed to component or circuit faults, or selection of materials.

The degree of bond strength of the components to the board is also dependent on the quality of the chip termination, its own intrinsic strength, solderability and resistance to solder leach, as well as the selection of solder.

Defects of misaligned parts or units which rotate vertically to the board, to stand on end, (referred to as "tombstoning") can occur more easily with small chips, such as 0402 or 0805, and be process or material dependent. Too rapid a temperature rise in the IR or vapor phase reflow cycle can cause sudden outgassing of solder pastes, dislodging the component off its circuit pad. Also, chips with end terminations of dissimilar solderability, due to tarnishing or contaminants, or leaching of the metallization, or, pad dimensional variations, can create preferential wetting on one end of the device; the solder surface tension may pull the unit up on end, or off at an angle to create an open circuit. The same phenomenon can occur if the circuit pad terminals exhibit the same variability, or excessive solder is applied to one end of the device.

The industry has developed "barrier" type terminations for chip capacitors with superior properties, namely solderability and leach resistance which has optimized the product for these attachment processes. Refer to sections 0-3 and 0-4 for details on barrier terminations, and selection of solder types.

Epoxy Bonding

Nonconductive thermosetting epoxies are utilized to affix the capacitor body to the substrate, in preparation for secondary electrical connection, either by soldering (solder reflow or solder wave) or by wire bonding (ultrasonic or thermal-compression bonding).

An electrical mechanical bond, analogous to soldering of chips, can be achieved by using conductive epoxies, which contain metal powders of silver, copper or aluminum. Epoxies require a low temperature cure in the range of 25°C to 150°C.

Wire Bonding

Wire bonding methods involve welding of very thin gold or aluminum wires to components, to effect an electrical connection; physical attachment of the capacitor body to the substrate must be made by other means, such as epoxy bonding. The wire bond to the chip metallization or substrate pad is attained with heat and pressure, applied to the fine diameter (.001') wire tip. Localized heat at the bond is applied from an external source, as in thermal-compression bonding, or by pulsation of the wire tip, as in ultrasonic bonding. In both cases, the heat and pressure result in intermetallic mingling of the wire and host material, effecting a bond.

THERMAL PROPERTIES OF CHIP CAPACITORS

Chip attachment methods invariably involve thermal cycling of the component. The expansion characteristics of the chip and substrate, as well as the mechanical properties of the bonding medium result in residual stresses, the degree of which determine the reliability of the bonded chip.

Chip capacitors can tolerate relatively high temperatures, by virtue of their processing, which typically involves a 1100°C to 1200°C firing of the dielectric body, followed with a second firing of the end metallization at approximately 850°C. Chips therefore could be cycled to as high as 850°C with no detrimental effect on the devices, provided the process does not expose the product to sudden or nonuniform temperature changes, which can cause thermal shock failure. Capacitors with nickel barrier terminations, which have a solder coat over the nickel, (or solder coated terminations) are restricted to the reflow temperature of the solder.

Temperature cycling causes a change in the mean interatomic spacing of the atoms in the crystal lattice, due to variations in thermal energy. The characteristic dimensional change of materials with temperature is a function of temperature, and is reported as the volumetric or linear coefficient of thermal expansion, expressed as:

$$(\text{linear coefficient}) \propto = dl/IdT \text{ (cm/cm/°C, or in/in °C)}$$

If the dimensional changes caused by temperature cycling are not uniform, the resultant differential strains cause stresses within the material. These stresses are significant in ceramic materials, which, unlike metals, lack ductility to relieve the stress. Heating of a material causes a positive expansion, resulting in compressive stress. Conversely, cooling results in tensile forces, as the material attempts to contract. As ceramics are characteristically weaker under tensile load, it follows that the type of temperature change, i.e. heating or cooling, as well as the rate, uniformity and degree of change are critical. Thermal cycling of chip capacitors therefore involves the following general precautions:

The rate of heating must be uniform and controlled to preclude the occurrence of differential strains in the chip, as is accomplished in a reflow furnace. Other soldering methods, such as hand or wave soldering should be preceded with a preheat cycle to bring the components to the solder flow temperature gradually. Although heating generally produces the more benign compressive stresses in the ceramic body, it should be noted that the more heat conductive chip end metallizations heat preferentially, i.e., the chip ends expand more rapidly than the main body of the chip, resulting in tensile stresses between the body and metallized ends.

Chip capacitors are even more vulnerable to failure during the cooling cycle, as negative temperature gradients cause primarily tensile stress. Cooling must therefore be gradual and uniform, with no localized forced cooling or contact of the chip with any efficient heat sink.

The effects of capacitor geometry are self evident; thermal gradients and resultant stresses are directly proportional to chip mass, hence larger units are more susceptible to thermal shock than smaller devices. Also, the contribution of preferential heat conduction of end terminations to undesirable stresses increases with larger or longer chips, as more mass is available to maintain the thermal gradients.

Without mechanical restriction, thermally induced stresses are released once the capacitor attains a steady state condition, at any given temperature. Capacitors bonded to substrates, however, will retain some stress, due primarily to the mismatch of expansion of the component to the substrate; the residual stress on the chip is also influenced by the ductility and hence the ability of the bonding medium to relieve the stress. Unfortunately, the thermal expansions of chip capacitors differ significantly from those of substrate materials. At 25°C to 300°C, capacitors typically range in expansion coefficient from 8.3 x 10^{-6} to 12.2 x 10^{-6} in/in/°C, while 99% Alumina is approximately 6.0 x 10^{-6} in/in/°C and P.C. board is typically 16.0 x 10^{-6} in/in/°C.

Chips bonded to alumina therefore will retain a tensile stress, as the expansion coefficient of the dielectric material exceeds that of the substrate. On cooling, the chip capacitor will attempt to shrink more than the substrate, but is restrained from doing so by the substrate material and solder or epoxy bond. Chips bonded to P.C. board will retain a compressive stress, as the substrate material attempts to shrink more than the chip. In either case, a shear stress is incorporated into the bond medium; the reliability of the bond therefore is greatly dependent on the load bearing capability of the bonding material.

SELECTION OF SOLDER

Solders are the most common bonding alloys used in capacitor attachment. 'Low temperature'

solders, with flow points under 250°C, are generally tin-lead alloys, with or without silver additions. 'High temperature' solders, with flow points of 260°C to 370°C are based on high lead content, alloyed with silver and/or tin, or based on gold, alloyed with germanium or tin.

Solders are selected based on the assembly temperature restrictions of the circuit, the hardness or ductility of the alloy, and the comparability of the solder to the chip termination and substrate conductor composition. Common solder types, flow points and hardness are tabulated in Table 0-1. Of importance are the following considerations:

Solder Leach: At the solder flow temperature, tin-lead alloys absorb silver (or gold) from the chip termination and/or the substrate pad. This effect is minimized by using solders which contain some percentage of silver, such as Sn62, and by limiting the time at reflow temperature to the minimum required to obtain good wetting and a well rounded fillet (approximately 5 seconds). Excursion of temperature above the flow point of the solder need also be avoided, as the leaching rate increases rapidly with temperature. The leaching effect is cumulative; repeated reflow of the solder during processing of the circuit will aggravate the problem.

Capacitor termination alloys and geometry are designed to reduce the leaching effects of solders. Termination materials have evolved from pure silver to silver-palladium alloys, typically 80Ag-20Pd, as the palladium inhibits silver leaching. Leaching, if it occurs, is predominant at the corners and edges of the chip termination, where the termination alloy is thinnest. This effect is minimized by the chip manufacturer by rounding of the corners and edges of the chip, with a tumbling process, before terminations are applied, to obtain a more uniform thickness of coverage.

Vapor phase reflow, and dual wave soldering, utilized with surface mount technology, have imposed solder leach requirements on components which preclude the use of silver-palladium terminations. Best resistance to solder heat is attained by the use of barrier type terminations, which have a nickel layer plated over a silver termination, with a solder or tin protective overcoat, to enhance solderability and prevent oxidation of the base metal layer. Capacitors with such terminations will survive molten solder at 260°C, with no discernible leaching effect, for several minutes, versus less than twenty seconds for the best Pd-Ag alloys, as nickel is relatively insoluble in Sn, Pb or Ag, and therefore acts as a barrier to solder leaching.

Solder Hardness: As described previously, thermal expansion mismatch of the chip capacitor and the substrate material results in residual shear stress at the bond. Theoretical calculations indicate that this stress can exceed 7000 psi, sufficient to lead to rupture of the chip, if the latter is under tension, or failure of the bond, if the chip is under compression. Fortu-

nately, this condition is alleviated by the ability of the bonding alloy to deform and absorb the majority of the stress. The ductility of the solder alloys is inversely proportional to the hardness of the material, hence use of softer solders (of lower Brinell hardness) is desirable.

The most common solder used in hybrid circuit application is Sn62 (62Sn,36Pb,2Ag). Selection of other solders is often predicated on the need for higher temperature tolerance of the circuit, i.e., bonding alloys with higher flow points are mandatory.

TABLE O-1
COMMON BONDING ALLOYS

Solder Type	Flow Point °C	Brinell Hardness
Sn63 (63Sn, 37Pb)	183	30
Sn60 (60Sn, 40Pb)	189	28
Sn62 (62Sn, 36Pb, 2Ag)	189	33
Sn50 (50Sn, 50Pb)	212	24
95Sn, 5Ag	240	22
80Au, 20Sn	280	115
Sn5 (95Pb, 5Sn)	312	15
88Au, 12Ge	356	107
95Pb, 5Ag	360	12

CHIP TERMINATIONS

Capacitor terminations consist of metal-frit (glass) compounds which are fused to the capacitor body, to effect an electrical connection between the internal capacitor electrodes and the circuit pads. Terminations can be classified into two general categories: older thick film silver or silver-palladium (80Ag-20Pd) metallizations, and the more popular barrier type termination used for surface mount components.

The silver-palladium termination has adequate resistance to solder leach, and less tendency to tarnish than pure silver terminations. Silver finds application mostly on units destined for axial or radial leading, or on specialty items, such as high voltage capacitors, which require the use of more ductile silver metal to reduce thermal shock hazards to these units when leaded.

Silver bearing terminations can tarnish. Usually packed with a tarnish retardant paper, capacitors will store indefinitely and solder properly with the appropriate fluxes. Severely tarnished units can be restored to a clean metal finish by refiring of the product to approximately 700°C to 800°C. Note that product supplied in reeled format cannot be effectively protected by tarnish retardant paper, as units stored in bulk, hence inventory planning or the use of barrier termination is recommended.

Barrier layer terminations are based on plating technology to provide 100 to 150 microinches of nickel thickness over a fired silver termination. As nickel readily oxidizes, a second tin/solder or tin layer 200 to 250 micro inches thick is plated over the nickel, to protect it and provide a readily solderable surface with good shelf life.

The electrolytic process is perhaps the preferred method of nickel deposition. A current is utilized to deposit nickel from nickel sulfamate and nickel chloride in a boric acid solution onto the silver termination of the capacitor. This termination differs from conventional materials in that the frit which bonds the termination to the capacitor must be chemically resistant to the plating solutions, and thus is bismuth free. (Such frits do not promote solderability, hence units with this termination are unsolderable unless properly plated with nickel and solder). Immediately after the nickel process, units must undergo the solder process before the onset of any oxidation of the base metal layer. Units are electroplated using tin and lead concentrates in a deionized water solution.

An electroless method of nickel deposition, based on chemical reduction of nickel boron solutions and catalytic activators, can also provide a continuous nickel barrier layer, but is not as suitable for tin lead plating. Alternate application of a solder coat by wave soldering methods creates dimensional tolerance difficulties, not desirable for components to be taped and reeled for use in surface mount technology

The distinct advantage of the nickel barrier termination is evident in its name; it serves not only as a guard against solder leach, by virtue of the relatively insoluble nature of nickel in solder alloys, but also forms a barrier to the formation of intermetallic compounds in the solder joint which can adversely affect the long term reliability of the bond. Non barrier terminations can be affected by a time dependent diffusion phenomenon of Ag, Pd and Sn atoms, which accelerate with thermal cycling, and can eventually lead to alteration of the physical properties of the bond, and result in stress cracks separating the component from the assembly. Capacitors with nickel barrier terminations have been shown to arrest the diffusion process and the formation of intermetallic compounds, hence maintaining the integrity of the bond.

The quality of capacitors with barrier terminations is largely dependent on the properties of the ceramic dielectric and the process parameters used for plating. Not all dielectric materials, terminations and plating solutions are entirely compatible, and great care must be exercised by the manufacturer to produce product with suitable electrical and mechanical properties. The plating processes, for example, may alter the dielectric surface, and affect the insulation resistance of the product. Also, the rate of nickel deposition and plating bath chemistry and temperature can establish a certain intrinsic stress in the nickel layer. Despite the thin dimension of this layer, the nickel may impart a significant tensile stress on the unit at the termination which can lead to mechanical failure, usually occurring shortly after soldering of the unit to the substrate. This phenomenon has manifested itself

primarily with the more susceptible X7R and Z5U formulations. Although it is a characteristic of all nickel deposition to retain a contractile or tensile condition, the industry has developed the methods to plate the material with controlled metallographic structure and ductility, to produce physical and mechanical properties suitable for all the dielectric types of multilayer capacitors.

Ion Migration

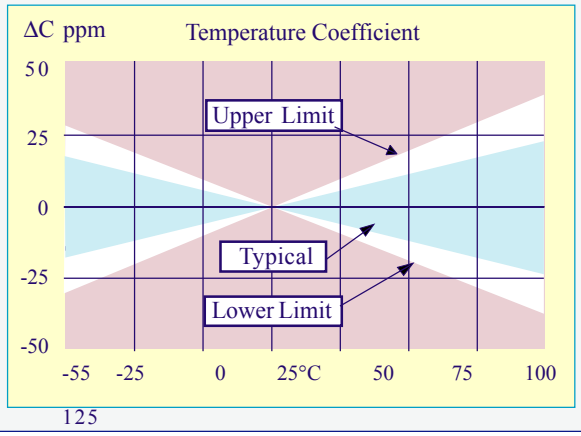
Chip terminations and bonding alloys contain metals, notably silver and tin, which can hydrolyze in the presence of water moisture. Under the influence of an electric field, the hydroxide can dissociate to form metal cations, which have a net positive charge, and can migrate to the cathode. This phenomenon occurs with AC voltage as well as with a dc bias, the severity of which is directly proportional to the voltage gradient. Given enough time, a bridge of silver or tin will form between chip terminations, reducing the insulation resistance and eventually forming an electrical short. Avoidance of this problem can be accomplished with the use of very expensive gold terminations and substrate conductors, or with the elimination of water moisture from the circuit, which precludes the formation of mobile cations. The latter is accomplished by hermetic sealing of circuits, or the use of water proof encapsulants, such as epoxies.

PERFORMANCE SPECIFICATIONS

Choice of capacitor type, other than size, value and termination, is based on dielectric performance characteristics. Following are tables and illustrations describing the dielectric characteristics of the popular Class I (NPO-COG) and Class II formulations (X7R, Z5U, Y5V).

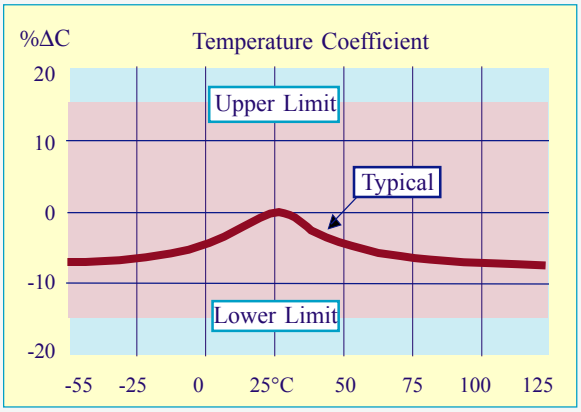
DIELECTRIC CHARACTERISTICS - COG

Operating Temperature Range:	-55°C to 125°C
Temperature Coefficient:	0 +/- 30 ppm/°C
Dissipation Factor:	.001 (0.1%) max @ 25°C
Insulation Resistance, 25°C	>100GΩ or >1000ΩF
125°C	>10GΩ or >100ΩF
Dielectric Withstanding Voltage:	<200V, 250%
* Whichever is greater	201-500V,150% or 500V*
	>500V, 120%, or 750V*
Aging Rate:	0% per decade
Test Parameters:	1KHz, 1.0 +/- 0.2 Vrms, 25°C
	1MHz for Capacitance <100pF



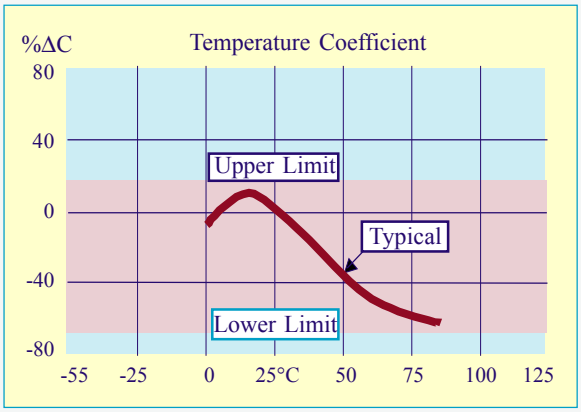
DIELECTRIC CHARACTERISTICS - X7R

Operating Temperature Range:	-55°C to 125°C
Temperature Coefficient:	+/-15% ΔC Max.
Dissipation Factor:	.025 (2.5%) max @ 25°C
Insulation Resistance, 25°C	>100GΩ or >1000Ω F
125°C	>10GΩ or >100Ω F
Dielectric Withstanding Voltage:	<200V, 250%
* Whichever is greater	201-500V,150% or 500V*
	>500V, 120%, or 750V*
Aging Rate:	< 2.0% per decade
Test Parameters:	1KHz, 1.0 +/- 0.2 Vrms, 25°C



DIELECTRIC CHARACTERISTICS - Z5U

Operating Temperature Range:	+10°C to 85°C
Temperature Coefficient:	+22%-56% ΔC Max.
Dissipation Factor:	.030 (3.0%) Max @ 25°C
Insulation Resistance, 25°C	>10GΩ or >100ΩF
Dielectric Withstanding Voltage:	<200V, 250%
	250V, 150%
Aging Rate:	~ 2.0% per decade
Test Parameters:	1KHz, 0.5 +/- 0.2 Vrms, 25°C



DIELECTRIC CHARACTERISTICS - Y5V

Operating Temperature Range:	-30°C to 85°C
Temperature Coefficient:	+22%-82% ΔC Max.
Dissipation Factor:	.050 (5.0%) max @ 25°C
Insulation Resistance, 25°C	>10GΩ or >100ΩF
Dielectric Withstanding Voltage:	<200V, 250%
	250V, 150%
Aging Rate:	~ 2.0% per decade
Test Parameters:	1KHz, 0.5 +/- 0.2 Vrms, 25°C