Technical Summary

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Technical Information

Novacap provides application notes throughout this catalog as a guide to chip selection and attachment methods. Refer to the Novacap Technical Brochure found at www.novacap.com for more details. This technical information includes the nature of capacitance, dielectric properties, electrical properties, classes of dielectrics, ferroelectric behavior, test standards, and high reliability test plans. Please do not hesitate to contact the sales office for any product or technical assistance.

Capacitor Size

Size availability is based primarily on capacitance values and voltage rating. Smaller units are generally less expensive. Because mass affects the thermal shock susceptibility of chip capacitors, size selection should consider the soldering method used to attach the chip to the board. Sizes 1812 and smaller can be wave, vapor phase, or reflow soldered. Larger units require reflow soldering.

Chip Selection

Multilayer capacitors (MLC) are categorized by dielectric performance with temperature. The Temperature Coefficient of Capacitance describes the variance of capacitance value with temperature. The choice of components is therefore largely determined by the temperature stability required of the device and the size necessary for the desired capacitance value and voltage rating.

Packaging

Units are available reeled, in waffle pack, or bulk packaged. Bar coded labels are standard for reeled and bulk packaging.

Primary Dielectric Types

C0G/NP0:

Ultra stable Class I dielectric, with negligible dependence of capacitance on temperature, voltage, frequency, and time. Used in circuitry requiring very stable performance.

X7R:

Stable Class II dielectric, with predictable change in properties across a temperature range of -55°C to +125°C. Used as blocking, decoupling, bypassing, and frequency discriminating elements. This dielectric is ferroelectric and provides higher capacitance than Class I materials.

BX:

The military specification for ceramic chip capacitors (MIL-PRF-55681) defines a mid-K stable dielectric designated as BX. The BX specification has voltage temperature limits in addition to temperature limits of capacitance. The BX dielectric is limited to ±15% maximum change in capacitance between 25°C and -55°C or +125°C and also has a voltage restriction of +15% / -25% maximum change in capacitance between 25°C and -55°C or +125°C at rated voltage.

Dielectric Termination Combinations

Dielectric	Code	Palladium Silver	Palladium Silver RoHS	Solderable Palladium Silver RoHS	Nickel Barrier 100% tin RoHS	Nickel Barrier 90/10% tin/lead	Nickel Barrier Gold flash RoHS	FlexiCap™/Nickel Barrier 100% tin RoHS	FlexiCap™/Nickel Barrier 90/10% tin/lead	Copper Barrier 100% tin RoHS	Copper Barrier 90/10% tin/lead	Solderable Silver RoHS
		P	PR	K	N	Y	NG	C	D	B	E	S
C0G/NP0	N/RN	•	•	•	•	•	•	•	•			•
R3L	K	•	•	•	•	•	•	•	•			
X7R	B/RB	•	•	•	•	•	•	•	•			•
X5R	W				•	•	•					
BX	X	•	•	•	•	•	•	•	•			•
C0G/NP0 (Mag free)	M	•	•	•						•	•	
X7R (Mag free)	C	•	•	•						•	•	
X8R	S	•	•	•	•	•		•	•			•
C0G/NP0 (160°C)	F	•	•	•	•	•		•	•			•
C0G/NP0 (200°C)	D			•								•
Class II (160°C)	G	•	•	•	•	•		•	•			•
Class II (200°C)	E			•								•
Pulse Power	P	•	•	•								
R2D	R	•	•	•								

Termination Material

We recommend the following termination types:

Solder Attachment:

N Nickel Barrier, 100% matte tin plated - RoHS

C FlexiCap™ with Nickel Barrier, 100% tin plated - RoHS

Y Nickel Barrier, tin-lead plated

D FlexiCap™ Nickel Barrier, tin-lead plated

B Copper Barrier 100% matte tin plated - RoHS

E Copper Barrier, tin-lead plated

K Solderable Palladium Silver - RoHS (suitable for conductive epoxy attach also)

S Solderable Silver - RoHS

Conductive Epoxy attachment:

P Palladium Silver

PR Palladium Silver - RoHS

NG Nickel Barrier Gold Flash, also suitable for soldering attachment - RoHS

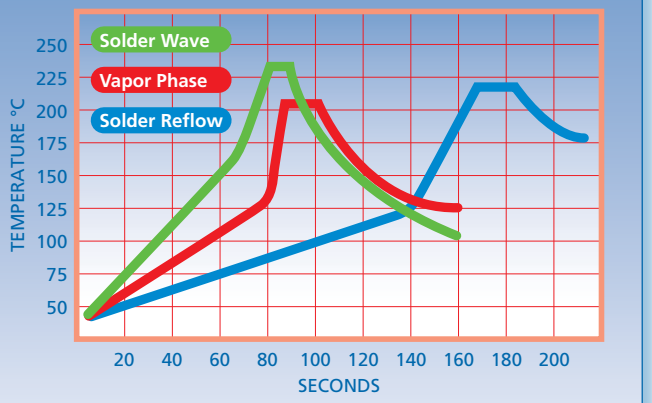
Bonding of capacitors to substrates can be categorized into two methods, those involving solder, which are prevalent, and those using other materials, such as epoxies and thermo-compression or ultrasonic bonding with wire.

The amount of solder applied to the chip capacitor will influence the reliability of the device. Excessive solder can create thermal and tensile stresses on the component which could lead to fracturing of the chip or the solder joint itself. Insufficient or uneven solder application can result in weak bonds; rotation of the device off line or lifting of one terminal off the pad (tombstoning).

There are practical limitations on capacitor sizes that prohibit reliable direct mounting of chip capacitors larger than 2225 to a substrate. Without mechanical restriction, thermally induced stresses are released once the capacitor attains a steady state condition, at any given temperature. Capacitors bonded to substrates, however, will retain some stress, due primarily to the mismatch of expansion of the component to the substrate; the residual stress on the chip is also influenced by the ductility and hence the ability of the bonding medium to relieve the stress. Unfortunately, the thermal expansions of chip capacitors differ significantly from those of substrate materials. At 25°C to 300°C, capacitors typically range in expansion coefficient from 8.3 x 10-6 to 12.2 x 10-6 in/in/°C, while 99% Alumina is approximately 6.0 x 10-6 in/in/°C and P.C. board is typically 16.0 x 10-6 in/in/°C.

Soldering

The volume of solder is process and board pad size dependent. Soldering methods commonly used in the industry, and recommended, are Reflow Soldering, Wave Soldering, and to a lesser extent, Vapor Phase Soldering. All these methods involve thermal cycling of the components and therefore the rate of heating and cooling must be controlled to preclude thermal shocking of the devices. In general, rates which do not exceed 120°C per minute and a T spike of 100°C maximum for any soldering process on sizes 1812 and smaller is advisable. Other precautions include post soldering handling, primarily avoidance of rapid cooling with contact with heat sinks, such as conveyors or cleaning solutions.



Recommendations

Preheat/Cooling rates not to exceed 120°C /minute with ΔT spikes to max temperature not to exceed 100°C for 1812 size and smaller.

Wave Soldering exposes the devices to a large solder volume; hence the pad size area must be restricted to accept an amount of solder which is not detrimental to the chip size utilized. Typically the pad width is 66% of the component width, and the length is .030" (.760 mm) longer than the termination band on the chip. For example, an 0805 chip which is .050" wide and has a .020" termination band therefore requires a pad .033" wide by .050" in length. Opposing pads should be identical in size to preclude uneven solder fillets and mismatched surface tension forces which can misalign the device. It is preferred that the pad layout results in alignment of the long axis of the chips at right angles to the solder wave, to promote even wetting of all terminals. Orientation of components in line with the board travel direction may require dual waves with solder turbulence to preclude cold solder joints on the trailing terminals of the devices, as these are blocked from full exposure to the solder by the body of the capacitor.

Restrictions in chip alignment do not apply to Solder Reflow or Vapor Phase processes, where the solder volume is controlled by the solder paste deposition on the circuit pads. Novacap has adopted the IPC-SM-782 methodology for solder reflow land patterns. The Novacap recommended solder pads brochure is available for reference on our website. Large chips are more prone to thermal shock as their greater bulk will result in sharper thermal gradients within the device during thermal cycling. Units larger than 1812 experience excessive stress if processed through the fast cycles typical of solder wave or vapor phase operations. Solder reflow is most applicable to the larger chips as the rates of heating and cooling can be slowed within safe limits.

Attachment using a soldering iron requires extra care, particularly with large components, as thermal gradients are not easily controlled and may cause cracking of the chip. Precautions include preheating of the assembly to within 100°C of the solder flow temperature; the use of a fine tip iron which does not exceed 30 watts and limitation of contact of the iron to the circuit pad areas only.

Bonding

Hybrid assembly using conductive epoxy or wire bonding requires the use of silver palladium or gold terminations. Nickel barrier termination is not practical in these applications, as intermetallics will form between the dissimilar metals. The ESR will increase over time and may eventually break contact when exposed to temperature cycling.

Cleaning

Chip capacitors can withstand common agents such as water, alcohol and degreaser solvents used for cleaning boards. Ascertain that no flux residues are left on the chip surfaces as these diminish electrical performance.