

Gain Slope issues in Microwave modules?

Physical constraints for broadband operation

If you are a microwave hardware engineer you most likely have had a few sobering experiences when you test your new design the first time, particularly wideband high frequency modules –they almost never look like the model. Many of the bigger issues come down to physics. Broadband modules e.g. 2 to 18 GHz virtually always have gain roll-off at the high end of the band, from a combination of transistor and package parasitic L's & C's give rise to gain roll-off and VSWR mismatch losses, while interconnect transmission lines have increasing loss with frequency.

To achieve good EW module signal fidelity over such frequency ranges requires thin dielectric interconnect substrates for:

- 1) Low ground via inductance for SMT amplifiers and RF components
- 2) 50 ohm line widths commensurate with SMT component signal pads
- 3) High isolation at high frequencies.

Further, any components in the RF signal path should have a signal contact width that closely matches the 50 ohm line width to prevent reflections (VSWR) which degrade signal fidelity. Typical construction has transmission line widths in the 0.010 to 0.02 inch line widths to achieve 50 ohm characteristic impedance. A consequence of module measured performance deviating from model prediction is an inability to pre-plan effectively to compensate for gain slope issues.

Gain equalizers, the historical approach

Historical implementation of gain equalizers utilized stacked combinations of a surface mount chip resistor with a surface mount chip capacitor. This results in a parallel R and C mounted across a gap in a microstrip line (i.e. connected in series on the transmission-line). By stacking the chips, the footprint on the circuit board is minimized to reduce VSWR reflection losses. Typical pick and place assembly and reflow methods want a pre-assembled stacked R || C. Typical SMT chip termination materials make it difficult to pre-attach the Resistor and capacitor chips without the connection reflowing, and possibly dis-assembling during board attach. The stacked assembly is on a small scale, the line width constraints noted above means that the R& C chips need to be 0201 or possibly as large as 0402 case sizes for good VSWR performance across EW bandwidths. Enough mechanics, the more important electrical impact from implementing equalizers with standard chip R's and C's is the parasitic circuit elements of such parts. We are all conditioned to think of leadless SMT chips as being the closest we can get to ideal circuit elements for high frequencies; once again ideal is a relative term. For comparison, see the graph in figure 1 below comparing the frequency response of an ideal parallel R-C, versus a typical stacked chip implementation. Most of the effect is due to the series self-inductance of the chip capacitor which

becomes series resonant with the capacitor giving rise to a rapid change in slope and greater variation between equalizers of the same design.

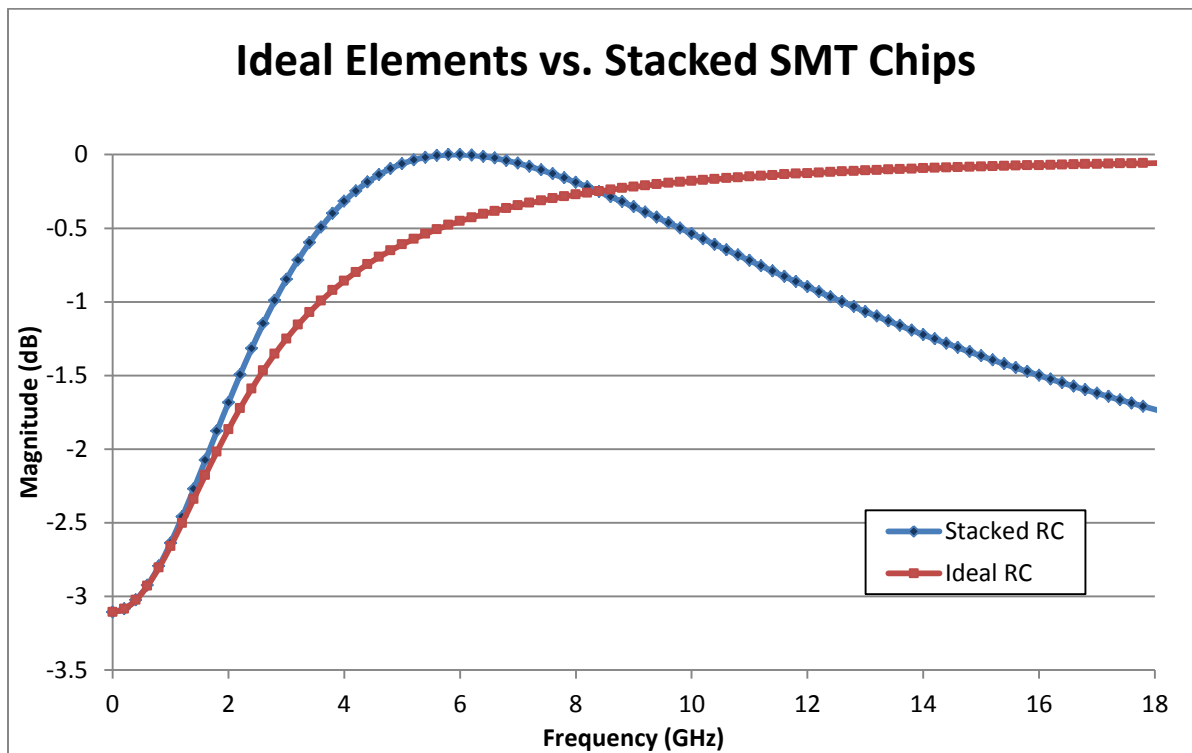


Figure 1

A new breed of Gain Equalizer

Dielectric Laboratories, Inc. (DLI) Gain Equalizers employ monolithic construction with precision thin film conductor and resistor films and proprietary high dielectric constant ceramics for superior RF performance repeatability. Integrated R and C values are realized to produce the desired gain slope. An EW series of equalizers add to the range of equalizers for applications ranging from 6 GHz to over 40 GHz. These are a small, low cost solution to your gain slope challenges. The EW series are 0.026 x 0.016 x 0.007 inches (smaller than 0302 case size), with terminations compatible with standard SMT or conductive epoxy attachment. Figure 2 below illustrates typical measured performance from 50 MHz to 20 GHz, for the 6 parts in the series with slopes ranging from nominally 1dB to 3.5dB.

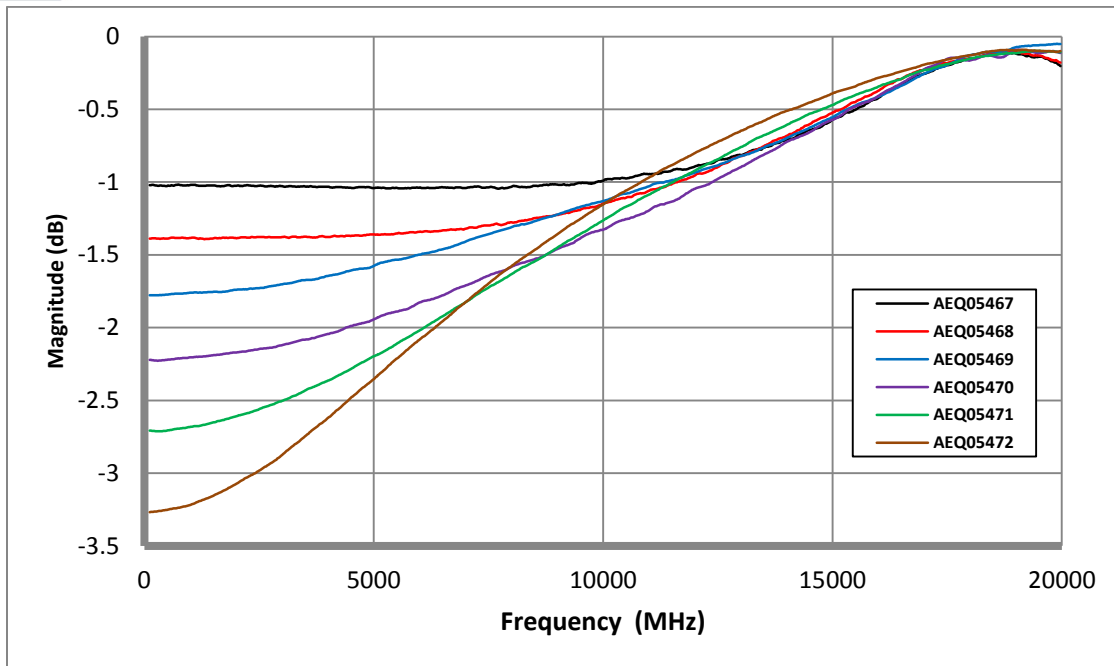


Figure 2

The performance shown is measured on a test coupon with a microstrip 50 ohm transmission line, with a trace width of 0.017 inches fabricated on 0.008 inch thick R04003 circuit board. Note that the part width is a good match to a 50 ohm line width for optimal broadband performance. Each part in the series is footprint interchangeable, making these parts easily interchangeable to optimize module gain flatness.

Engineering kits are offered which contain all 6 slope part types. Since no ground connection is required for DLI's gain equalizers, it is typically feasible to insert them into modules where no pre-planned provisions were made. In the case of a typical printed wire board all one needs is a steady hand and a utility knife to cut a nominal 0.010 inch gap in the transmission line, and then install the gain equalizer.

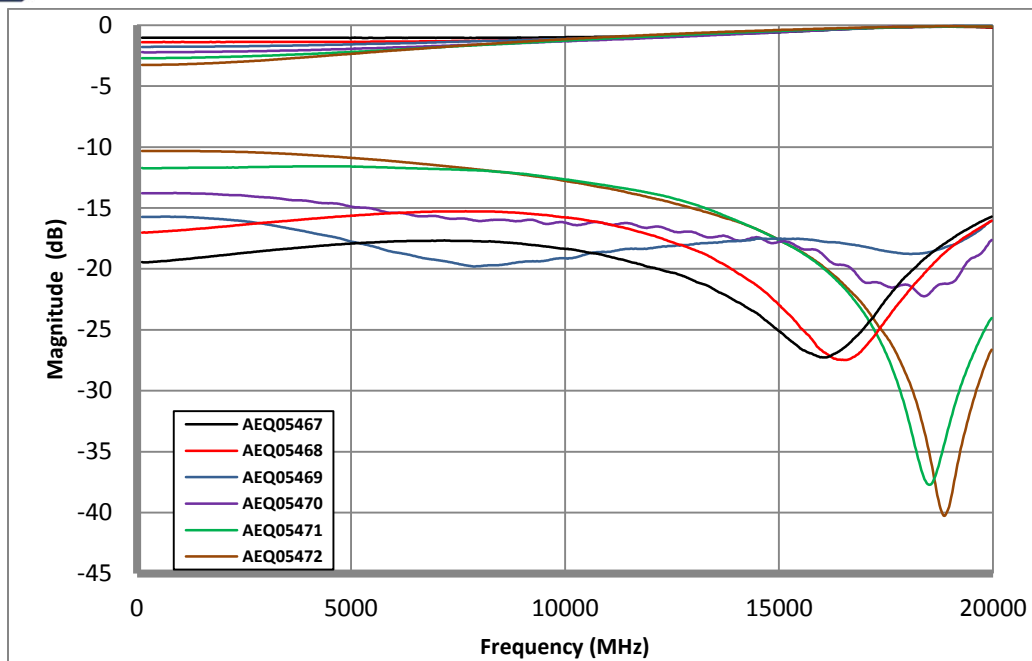


Figure 3

Figure 3 compares simulated return loss for parts with different gain slope values. Parts with higher gain slopes have lower return loss values at low frequencies, for example a part with 3.5dB gain slope has approximately 9 dB return loss at low frequencies, however the resistor’s attenuation behaves similarly to a “pad” so that VSWR interaction between adjacent circuit components is reduced.

When slope compensation needs are greater than an individual gain equalizer provides two other strategies should be considered; 1) use more than one equalizer and put an amplifier between them where the amplifier isolation will minimize the VSR interaction, 2) Utilize a length of 50 ohm transmission-line between the gain equalizers. Depending on the length of transmission line, the return loss can be improved considerably—in addition the composite gain slope can be further tailored to module needs. Figure 4 illustrates the concept showing performance for a short length of transmission line ~ 0.02 inches versus 0.25 inches between a pair of gain equalizers.

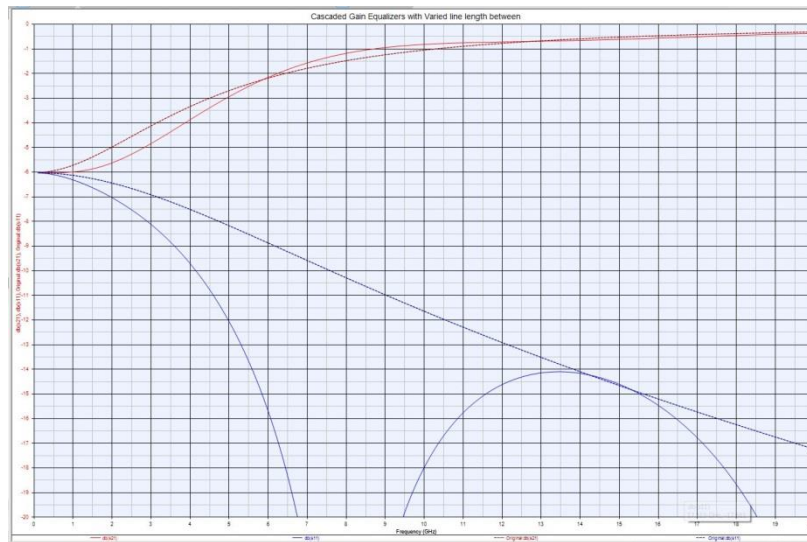


Figure 4

The gain equalizers are intended to be used in small signal applications, the limitation is principally thermal dissipation, a combination of very small part size and low thermal conductivity of printed wire board materials. The dissipated power will be greater for signals in the lower frequencies in contrast to the higher frequency end of the design range where the insertion loss reaches a typical value of 0.2 dB. Typical dissipated power limit is 30 mw or greater for baseplate temperatures up to 80° C.

Conclusion

If you have gain slope issues in your microwave modules you should consider this product. DLI gain equalizers can outperform alternative solutions in an easy to use form with excellent RF repeatability. The EW designer kit provides DC to 20 GHz performance with slopes from 1 to 3.5dB with a common footprint to simplify your prototyping needs.