Build to Print

Thin Film

Design Guide

PRECISION DEVICES

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USING THIS GUIDE

The Design Guide has been created to assist in the design of RF and Microwave circuits which utilize DLI's thin film ceramic materials and metal systems. This guide will also give an overview of the manufacturing processes and procedures. This document is intended to be used as a roadmap leading to successful product implementation.

AVAILABLE SUBSTRATE MATERIALS

The ceramic materials listed are manufactured in plate form for use in the fabrication of single layer capacitors, custom build to print products [parts designed by customers and manufactured using DLI thin film processes] and DLI designed thin film products. DLI originated thin film designs are only implemented using PI, PG, CF, and CG materials. SLC's may utilize any of the materials. PI, QZ, and AG are purchased from outside sources.

Class I Dielectric Materials - Single Layer Capacitor and Thin Film Products

DLI Class I Dielectric Materials								
Dielectric Code	**Material**	**Relative K**	**TCC -55°C to 125°C (ppm/°C Max)**	**1 MHz DF (% Maximum)**	**Typical Loss Tangent**	**25°C/125°C IR (MΩ)**	**Surface Finish (micro-inch)**	**CTE (ppm/°C)**
QZ	Quartz	3.82	-	0.15	0.000015@ 1 MHz 0.00033@ 24 GHz	$10^6/<10^5$	<0.1	0.55
AG	Aluminum Nitride (AlN)	8.6 (±0.35)	-	0.001	0.005@ 8GHz	$10^6/<10^5$	As Fired <20 Polished <2	4.6
PJ	96% Alumina	9.6	-	0.02	0.0004	$10^6/<10^5$	As Fired <45 Polished <1	6.4-8.2
PZ	99.5% Alumina	9.5	-	0.15	-	$10^6/<10^5$	As Fired <5 Polished <1	-
PI	99.6% Alumina	9.9	P105 ± 20	0.15	0.00018 @ 12GHz	$>10^6/<10^5$	As Fired <4 Polished <1	6.5-7.5
PG		13.3	P22 ± 30	0.15	0.00051 @ 12GHz	$>10^6/<10^5$	Polished <5	7.6
AH		20	P90 ± 20	0.15	-	$>10^6/<10^5$	Polished <5	9.6
NA		22	N30 ± 15	0.15	-	$>10^6/<10^5$	Polished <5	10.1
CF		25	0 ± 15	0.60	0.00028 @ 10GHz	$>10^6/<10^5$	Polished <5	9.0
CD		37	N20 ± 15	0.15	-	$>10^6/<10^5$	Polished <5	5.8
CG		67	0 ± 30	0.70	0.00087 @ 5GHz	$>10^6/<10^5$	Polished <5	9.0
NP		85	N750 ± 200	0.50	-	$>10^4/<10^3$	Polished <5	-
NR		160	N1500 ± 500	0.25	-	$>10^6/<10^5$	Polished <5	10.0
NS		300	N2400 ± 500	0.70	-	$>10^6/<10^5$	Polished <5	-
NU		600	N3700 ± 1000	1.50	-	$>10^6/<10^5$	Polished <5	-
NV		900	N4700 ± 1000	1.20	-	$>10^6/<10^5$	Polished <5	-

CHOOSING THE METAL SYSTEM

The choice of a metal system is governed by one or more of the following features.

- Filter mounting technique - solder - surface mount,
- Filter mounting technique - conductive epoxy mount,
- Vias and/or Castellations
- Insertion loss – conductor thickness, frequency of operation and skin depth.
- Line width and line spacing requirements.
- The requirement for integrated resistors.
- The current carrying requirements.

Basic Metals and Thin Film Circuit Function

Function	Type of Metal	Typical Thickness Range	Comments
Resistor	Tantalum Nitride (TaN)	12 to 200 Ohms/square	50 Ohms/square – standard. 25 to 100 Ohms/square – preferred.
Adhesion	Titanium Tungsten (TiW) Tantalum Nitride (TaN) Titanium (Ti)	300 to 600 Å 500 to 1200 Å 300 to 1000 Å	Titanium Tungsten is the primary adhesion layer material. Tantalum Nitride must be used with resistor designs. Titanium can be used with AlN and Pt
Barrier	Nickel (Ni)	40 to 100 µ”	Solderable metal system
Conductor	Gold (Au) Copper (Cu)	5 to 200 µ” 10 to 200 µ”	Fine line geometries available.
High Current Conductor	Gold (Au) Copper (Cu)	200 to 600 µ” 200 to 1000 µ”	3 mil traces +/- 0.4 mil tolerance. 5 mil traces +/- 0.5 mil tolerance.
Solder Attachment	Gold-Tin (AuSn)	150 to 325 µ”	Fine line geometries *not* available. Low quality geometry resolution.
Conductor / Barrier	Platinum (Pt)	6 to 10 µ”	Solderable metal system. Low quality geometry resolution.

Metallization Systems, Application, and Physical Parameters

Metallization System	Application	Component Attachment Method	Nominal Thickness Range & Resistor Layer	Comments	Max. Temp. °C (1)
Tantalum Nitride (TaN) Titanium Tungsten (TiW) & Gold (Au)	Standard Thin Film Metal System for Conductors With Resistor Layer	Au/Sn, Au/Si, Au/Ge – Eutectic Epoxy	TaN: 25 to 100 Ohms/square TiW: 300 to 500 Å Au: 5 to 300 µ”	Not Recommended for Tin/Lead Solder Attach. Compatible With Wire bonding – Maintain Gold Over 100 Micro inches for Wire bonding.	380
Titanium Tungsten (TiW) & Gold (Au)	Standard Thin Film Metal System for Conductors Without Resistor Layer	Au/Sn, Au/Si, Au/Ge – Eutectic Epoxy	TiW: 300 to 500 Å Au: 5 to 300 µ”	Not Recommended for Tin/Lead Solder Attach Compatible With Wire bonding– Maintain Gold Over 50 µ” for Wire bonding.	425
Tantalum Nitride (TaN) Titanium Tungsten (TiW) Nickel (Ni) & Gold (Au)	Standard Thin Film Metal System for Conductors Higher Durability With Resistor Layer.	Au/Sn, Au/Si, Au/Ge – Eutectic SN/Pb Epoxy	TaN: 25 to 100 Ohms/square TiW: 300 to 500 Å Ni: 40 to 100 µ” Au: 5 to 300 µ”	Compatible With Tin/Lead Solder Attach – Maintain gold 5 to 20 µ” maximum to minimize embrittlement.. When repeated soldering is required for repairs. Compatible With Wire bonding – Maintain Gold Over 50 µ”	350
Titanium Tungsten (TiW) Platinum (Pt) Gold (Au)		Au/Sn, Au/Si, Au/Ge – Eutectic, Sn/Pb Epoxy	TiW: 300 to 500 Å Pt: 6-10 µ” Au: 5 to 300 µ”	Compatible with Tin/Lead Solder attach – Maintain Gold 5-20 µ” for Solder Attach. When repeated soldering is required for repairs. Compatible with wire bonding – Maintain Gold ≥ 100 µ” for wire bonding.	
Titanium Tungsten (TiW) Nickel (Ni) & Gold (Au)	Standard Thin Film Metal System for Conductors Higher Durability Without Resistor Layer	Au/Sn, Au/Si, Au/Ge – Eutectic Sn/Pb Epoxy	TiW: 300 to 500 Å Ni: 40 to 100 µ” Au: 5 to 300 µ”	Compatible With Tin/Lead Solder Attach – Maintain Gold 5 to 20 µ” maximum to minimize embrittlement. When repeated soldering is required for repairs. Compatible With Wire bonding – Maintain Gold Over 50 µ”.	350
Tantalum Nitride (TaN) Titanium Tungsten (TiW) Gold (Au) Copper (Cu) Nickel (Ni) & Gold (Au)	High Current & Low Loss With Resistor Layer.	Au/Sn, Au/Si, Au/Ge – Eutectic Sn/Pb Epoxy	TaN: 25 to 100 Ohms/square TiW: 300 to 500 Å Au: 5 to 10 µ” Cu: 150 to 600 µ” Ni: 40 to 100 µ” Au: 5 to 300 µ”	Compatible With Tin/Lead Solder Attach – Maintain Gold 5 to 20 µ” maximum to minimize embrittlement.. When repeated soldering is required for repairs. Compatible With Wire bonding – Maintain Gold Over 50 µ”	350

Metallization System	Application	Component Attachment Method	Nominal Thickness Range & Resistor Layer	Comments	Max. Temp. °C (1)
Titanium Tungsten (TiW) Gold (Au) Copper (Cu) Nickel (Ni) & Gold (Au)	High current & Low Loss Without Resistor Layer	Au/Sn, Au/Si, Au/Ge – Eutectic Sn/Pb Epoxy	TiW: 300 to 500 Å Au: 500 to 1500 Å Cu: 150 to 600 µ” Ni: 40 to 100 µ” Au: 5 to 300 µ”	Compatible With Tin/Lead Solder Attach – Maintain Gold 5 to 20 µ”. When repeated soldering is required for repairs. Compatible With Wire bonding – Maintain Gold Over 50 µ”.	350
Titanium Tungsten (TiW) Nickel (Ni) & Gold Tin (AuSn)	For Gold/Tin Solder Systems.	Au/Sn	TiW: 300 to 500 Å Ni: 40 to 100 µ” AuSn: 100 to 350 µ”	Eliminates solder perform. Direct die attach to pad. (Au/Sn).	280
Notes 1 Intermittent for processing only.					

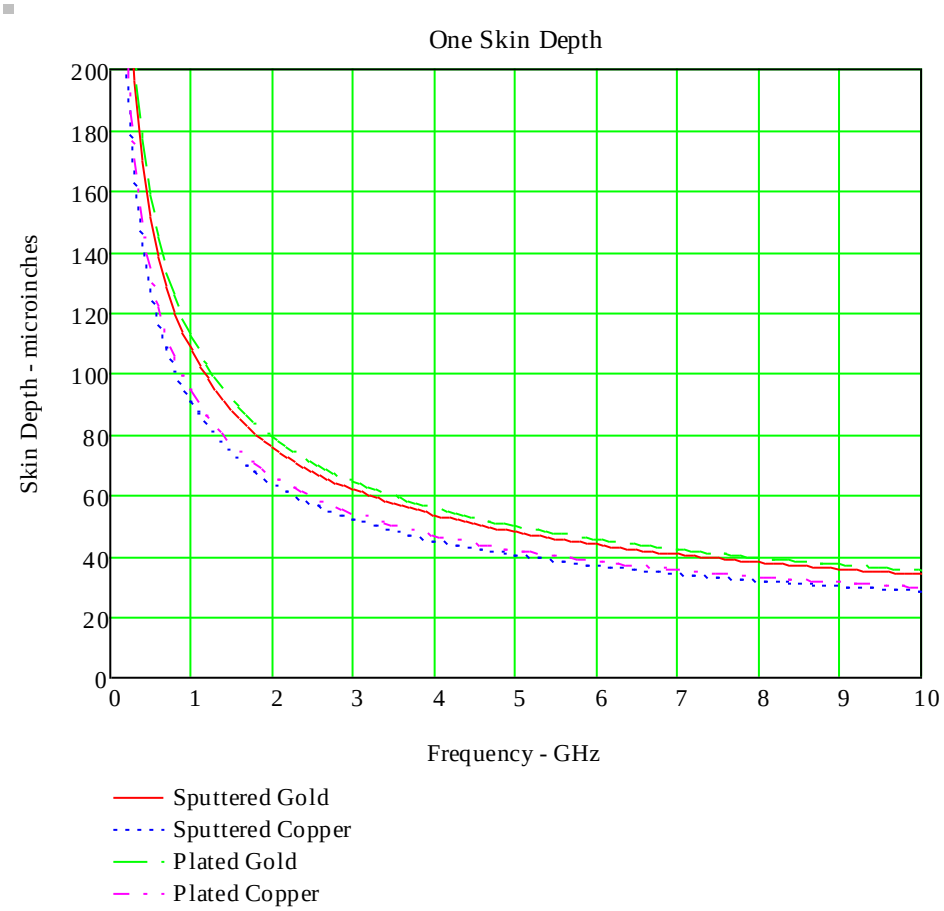
Metallization Systems

DLI Standard Metallization System			Application
S1	TiW 300 Å min., NiV 50µ”, Au 100 µ” min	Sputter Process	Solderable
S2	TiW 300 Å min., NiV 50µ”, AuSn 300 µ” min	Sputter Process	Solderable
S5	TiW 300 Å min., Au 100 µ” min	Sputter Process	Conductive epoxy attach wire bond interconnect
S5A	TiW 300 Å min., Au 200 µ” min	Sputter Process	Conductive epoxy attach wire bond interconnect
S10	TiW 300 Å min., Au 100 µ”, Ni 50 µ” min., Au 3-6 µ”	Sputter Process And Wet Plate	Solderable
S10A	TiW 300 Å min., Au 200 µ”, Ni 50 µ” min., Au 3-6 µ”	Sputter Process And Wet Plate	Solderable
S19	TaN 50 Ω/Square, TiW 300 Å min., Au 100 µ” min	Sputter Process	Resistors

Conductor Sheet Resistivity

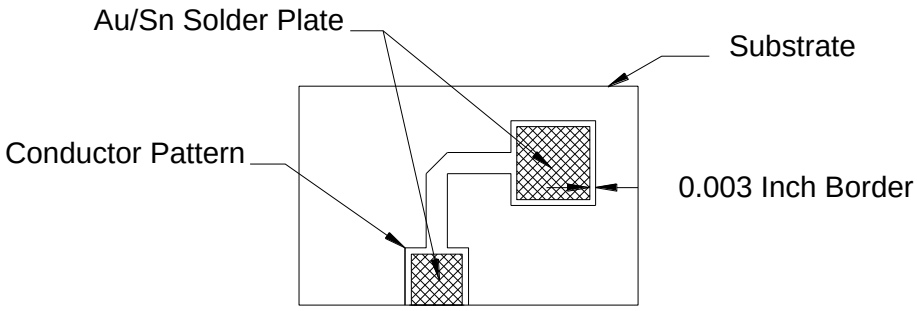
Sheet resistivity is typically 30 % higher with plated metal as compared to bulk resistivity of the same material and 20% higher with sputtered metal. See appendix for industry resistivity values.

The metallization layers and thickness is governed by the mounting strategy (ceramic circuit to next level part), insertion loss and current carrying requirements, the chip/component attachment process, and the input/output connections. The requirement for resistors will necessitate a metallization system that starts with an adhesion layer of tantalum nitride (TaN). Wire bonding to the gold (Au) surface of a circuit generally requires a minimum of 50 µ" of gold, although 100 µ" is recommended for most applications. When tin/lead soldering will be employed, a solderable barrier like nickel is required and the outer gold layer is used to prevent nickel oxidation and the thickness is minimized [5 to 20 µ"] to reduce solder embrittlement.



Gold-Tin Solder Offering

Gold-tin solder systems are employed in hybrid microelectronic applications for the mounting of semiconductor die to the parent circuit. Gold tin solder may be sputtered in selected areas of a circuit to facilitate component attachment. For areas within the substrate perimeter allow a 0.003 inch (0.076 mm) clearance to the border of the conductor to accommodate processing variation. This allowance is not required at the substrate edge.



Caution must be observed when exposing gold plated circuits to the elevated temperatures required to perform component attachment using solder. Prolonged exposure to elevated temperatures is sufficient to drive the underlying Ni barrier layer up through the gold, rendering the surface unbondable. Observe maximum temperatures listed in the tables. At 425 ^{o}C nickel can diffuse through 150 Microinches of gold in 15 minutes.

Also, surface concentrations of carbon on the gold surface can exceed 60% after the circuit has been put through a soldering operation. The maximum time at temperature and the duration have an impact on the ability to achieve acceptable wire bonds. It is recommended that plasma cleaning be employed prior to wire bonding.

FINE LINE CONDUCTOR FEATURES

The key to superior and repeatable performance in microwave structures is the control of the critical geometries of the metal features. Devices such as filters, diplexers, Lange couplers, directional couplers, interdigitated capacitors, and spiral inductors rely on the precision of the conductor line width and line spacing to achieve performance. The characteristic impedance of transmission lines is also governed by line widths. The coupling between transmission lines and the control of the even and odd mode impedance, to implement couplers and filters is governed by the line widths and the spacing between the adjacent transmission lines. The precise control of the spacing between the coupled lines ensures uniformity in VSWR and coupling necessary to make coupler and filter performance repeatable.

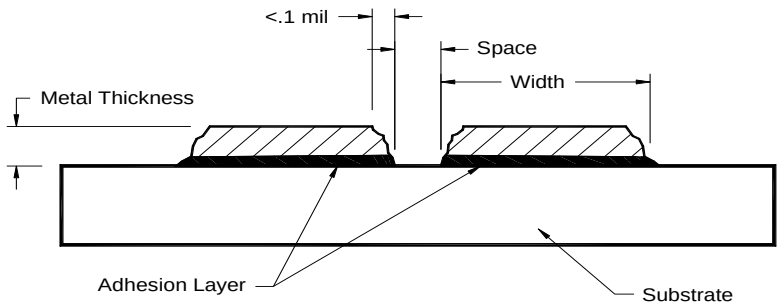
Minimum Line Width and Conductor Spacing Tolerance

Metal Layer	With Vias – Minimum Line Width/Spacing	Without Vias – Minimum Line Width/Spacing
Au (10 to 150 µ") (sputtered)	1.0	0.8
Au (150 to 300 µ") (sputtered)	1.5	1.0
Au (300 to 850 µ") (sputtered)	3.0	3.0
Cu (50 to 600 µ") (sputtered)	3.0	3.0
Cu (0.5 to 6 mils; Plated)	3.0	3.0
NiV (50 to 125 µ") (sputtered)	3.0	3.0

With the selection of the proper substrate/metallization system, excellent edge acuity can be achieved. The edge acuity is dependent on the thickness of the metal layers required, but generally is less than 0.1 mil.

Finished line widths will be within +/- 0.1 mils of the design dimension.

Fine line width and line space geometries are impacted by the quality of the ceramic surface. Some materials used in thin film products have grain structures and surface imperfections that may cause the loss of control of fine line widths and line space geometries. Polishing, which improves the quality of the surface, is also somewhat limited in that some materials do not hold up well to the forces created during polishing.
One material that is not as limited is polished alumina. The surface quality is good and 1 mil line width/spacing is possible and repeatable when vias are present and 0.75 mil line width/spacing is possible and repeatable when vias are not used.

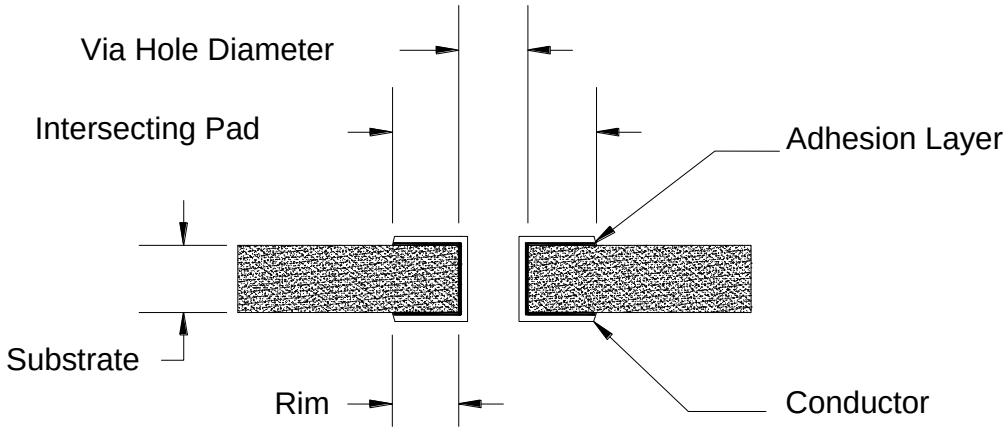


VIA DESIGN

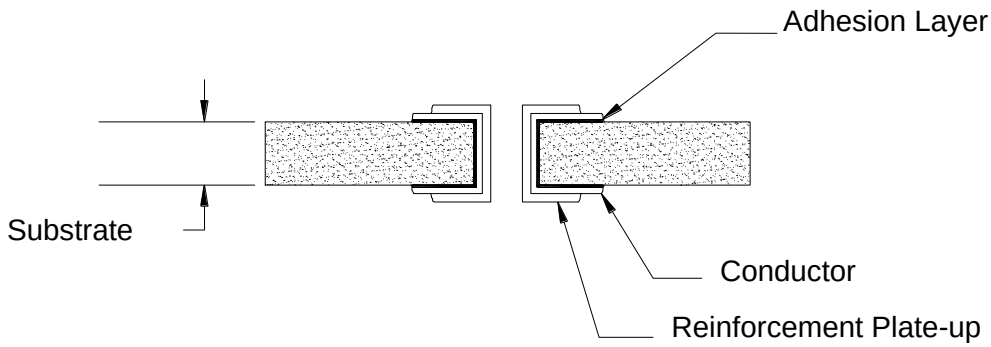
Plated Via Holes – Standard and Reinforced

The application of plated via's allows the design engineer to connect the circuit to the ground-plane.

Standard Via



Reinforced Via



Most applications which use plated via's find standard metal thickness through the holes acceptable. If higher currents are required, consider reinforcing the plated via. This may also be necessary to reduce RF loss in devices such as interdigital band pass filters.

This is done through a separate (additional processing) plating step in which DLI adds additional metal in and around the via to give better mechanical strength and lower via hole resistance. Refer to "Selective Plating Strategies" below.

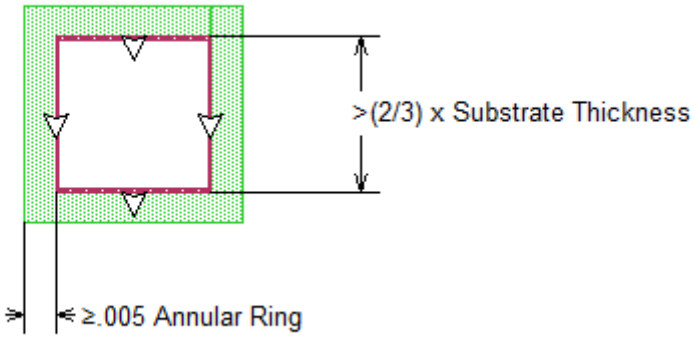
General Design Guidance for Vias and Castellations

Component	Limits and Recommendations
Substrate Hole Diameter	Absolute minimum; 50% of the substrate thickness and not less than 5 mils Recommended Minimum: 60% of the substrate thickness. Maximum: < 1.5 x substrate thickness
Minimum Rim (annular ring)	Minimum: 4 mils 2 mils for 10 mil thick Alumina Preferred: 5 mils or greater
Castellation rim I/Os	Minimum: 5 mils Preferred: 6 mils or greater
Via Corner Radius – square vias	Minimum: 3 mils. Preferred: 5 mils.

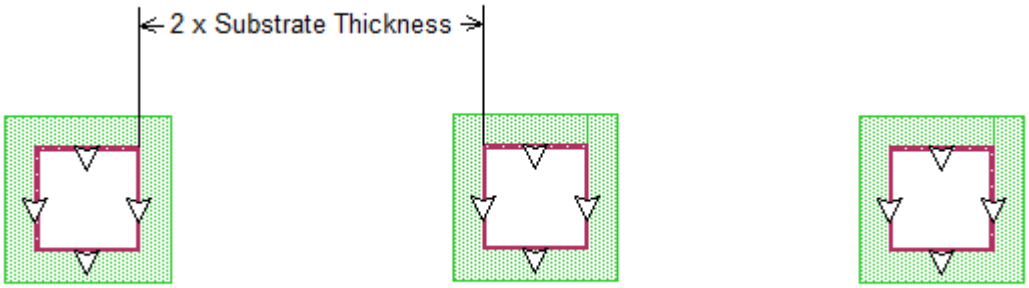
Recommended Plated Via Mechanical Requirements

Substrate Thickness inches (mm)	Substrate Hole Diameter inches (mm)	Minimum Intersecting Pad Size Inches (mm)	Minimum Via Spacing Center to Center inches (mm)	Minimum Via Spacing Center to Circuit Edge inches (mm)
0.005 to 0.012 (0.125 to 0.305)	0.005 to 0.020 (0.175 to 0.500)	Diameter + 0.010 (Diameter + 0.250)	0.030 or Diameter x 2.5 (Diameter + 0.500). Whichever is larger.	Diameter/2 + 2 x Substrate Thickness (Diameter/2 + 0.500)
0.015 (0.375)	0.009 to 0.100 (0.225 to 2.50)	" "	" "	Diameter/2 + 2 x Substrate Thickness (Diameter/2 + 0.500)
0.025 (0.625)	0.015 to 0.150 (0.375 to 3.750)	" "	" "	Diameter/2 + 1.5 x Substrate Thickness (Diameter/2 + 0.500)

Via Dimension



Via Proximity

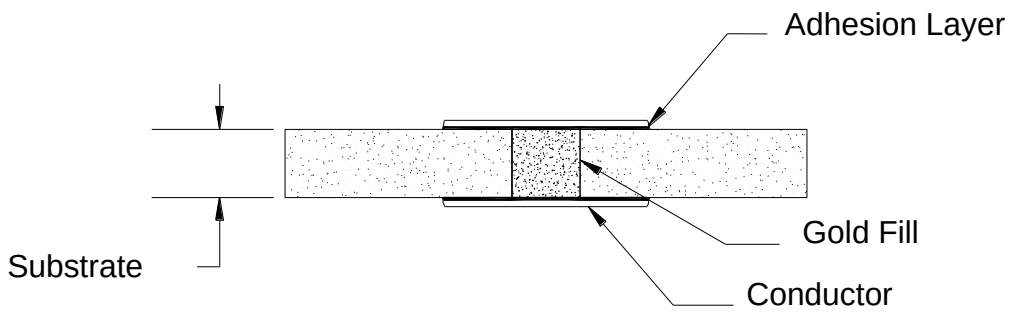


Filled Vias

Filled via's provide a good thermal path and ground return path from the top side conductors to the backside ground plane. In the case of mounting active die, the use of an array of filled via's effectively shunts heat away from the die. However, the technology is difficult to implement without issue and suffers from a significant processing cost penalty. When necessary, use gold fill for the via. Copper or silver filled via's can leach into other components of the metallization system, thereby leading to reliability problems.

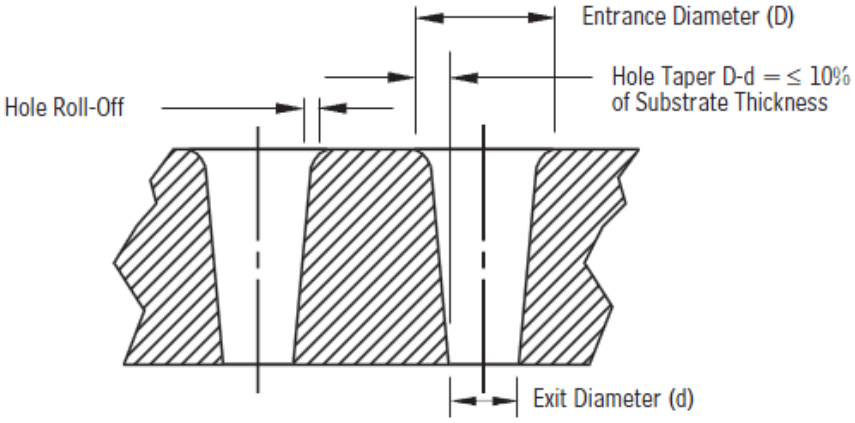
CTE mismatch between the ceramic and the metal in the via may create cracking issues.

Filled vias are not recommended for use unless a customer specifically requires the technology.



Via Taper

Laser drilling of via's will produce a taper from the entrance to the exit of the via hole.



Selective Plating Strategies

Selective plating is the application of different metal systems in different areas of a circuit or an additional plate up of the same metal in selected areas. Examples are the addition of a nickel metal layer in area where solder is required or to increase the metal thickness in vias or castellation walls without using nickel on the resonators of filters. Added metal, nickel, would be necessary in the I/O castellations and on the ground plane side of a filters for solder attach.

Many customers will only require 50 µ" of nickel and 3-6 µ" of gold. This 3-6 µ" of Au comes from the fact that this is the maximum thickness of gold that can be *electrolessly* plated. During electroless gold plating, the gold ions attach to the surface of the nickel, but the chemical process stops once the nickel surface is completely covered (the gold will not continue to plate onto itself). The disadvantage

to this process is that the plated gold thickness is restricted. However, the significant advantage of electroless plating over electrolytic plating is that the plating does not require an electrical charge to be flowing through the surfaces that need to be plated. I.e. isolated features will get plated.

Electrolytic plating has one major disadvantage. Electrolytic plating requires an electrical current to be flowing through the surfaces that need to be plated. This means that the plated surfaces need to have electrical continuity to the edges of the plate, since that's where the electrical terminals are attached during the process. Although, electrical continuity is typically not an issue for thin film filter designs. The major design advantage of electrolytic plating is that the plated gold thickness can exceed 3-6 μ", since gold can continuously plate onto itself as long as an electrical current is flowing through it and attracting the gold cations to the surface. These thicker gold plating schemes are required by some customers.

RESISTOR DESIGN GUIDELINES

DLI employs tantalum nitride (TaN) in the implementation of resistors This material has become the more widely accepted resistor material because of the higher maximum exposure temperature, the wider annealing window, and the superior resistance to harsh environments encountered in soldering and other processing.

The key design parameters that the engineer needs to be concerned with are: the resistor value, the stability with time and temperature, and power handling. The design of a thin film resistor is governed by the following equation:

$$R = \rho L / Wt$$

Where:
R = Total Resistance (Ω)
ρ = Bulk Resistivity of Resistor Material (Ω-cm)
L = Resistor Length (cm)
W = Resistor Width (cm)
t = Resistor Thickness (cm)

To ease design, a parameter known as sheet resistivity is provided. This term assumes L = W in the above equation so that:

$R_{sheet} = R_S = \rho / t$ (Ω/square). Therefore simply multiplying R_S by the Length (L) divided by the width (W) yields the actual resistance. $R_{Total} = R_{sheet}$ x Length (L)/Width (W)

The resist metallization layer for all the resistors on a given circuit is deposited in a single sputter operation. Thus, resistors on a single part must share the same resistivity. DLI typically uses 50 Ω per square for most work. Refer to the Standard Resistor Parameters table for electrical design parameters and allowable limits.

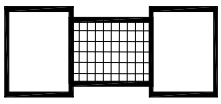
Standard Resistor Parameters

Thin Film Resistors	TaN
Available Sheet Resistivity's	12 to 200 Ω/sq., 50 to 100 Ω/sq. preferred
Temperature Coefficient of Resistance (-25 to 125 °C)	-75 to -100 (ppm/ °C)
Stability (Change after 1000 hours @ 125 °C)	0.02%
Short Term Exposure Max Temperature (2 minutes)	450 °C*
*If nickel in system, drop exposure temp to 350 °C	

There are two fundamental resistor layout techniques, the notched resistor implementation and the flush resistor process.

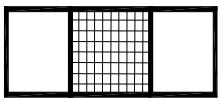
Notched Resistor Process

(Island method)



Flush Resistor Process

(Etch Back method)



The flush resistor is preferred due to ease of manufacturing and more consistent results.

Resistor Layout Guides

Parameter	Limit	Comments
Minimum Tolerance	1% (with laser trim)	10% standard, 20% preferred
Minimum Spacing Between Resistor Sections	0.001 inch	Serpentine Resistor Layouts
Minimum Length and/or	0.002 inch	Resistor Material

Width		
Minimum Conductor Pad Size	0.003 inch x 0.003 inch	
Conductor/Resistor Overlap	0.0005 inch per side	
Pre Trim Designed Value	-20%	Laser Trimmed Resistors
Nominal Sheet Resistance	25 – 100 Ohms/square	Preferred: 50 Ohms/square.

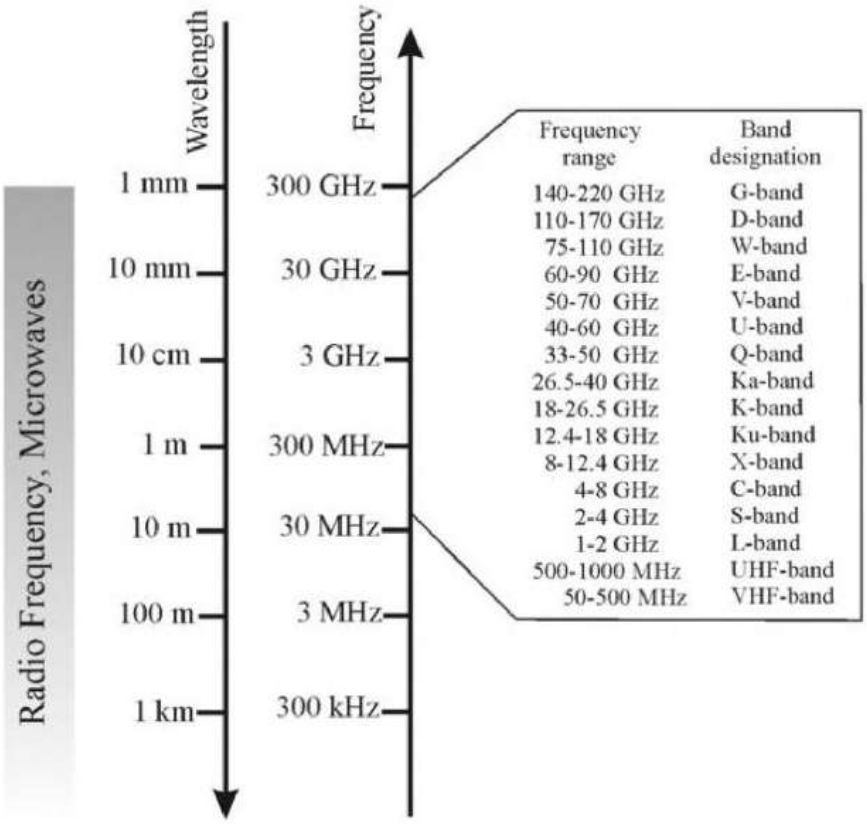
Dicing

Dicing or sawing the ceramic consists of cutting the individual component from the larger ceramic plate. This is accomplished with the use of diamond saws.

The standard tolerance on the component is +/- 1 mils. An enhanced tolerance of +/- 0.5 mils is possible but should be avoided if possible.

Appendix

RF / Microwave Spectrums



Typical Substrate Thickness Per Frequency Range

Material / Frequency	Alumina / PG	CF	CG
0.5~3 GHz	25 mil	20~30 mil	20~30 mil
3~6 GHz	25 mil	20 mil	20 mil
6~10 GHz	15 mil	15~20 mil	X
10~25 GHz	15 mil	15 mil	X
> 25 GHz	10 mil	10 mil	X

Bulk Resistivity

Silver	1.62 x 10^{-6} Ω-cm
Copper	1.7241 x 10^{-6} Ω-cm
Gold	2.44 x 10^{-6} Ω-cm0
Aluminum	2.688 x 10^{-6} Ω-cm
Platinum	10.58 x 10^{-6} Ω-cm
Palladium	10.8 x 10^{-6} Ω-cm
Nickel	6.9 x 10^{-6} Ω-cm
Titanium/tungsten	98 x 10^{-6} Ω-cm