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Capacitance Ageing of Ceramic Capacitors

Explanation of the natural ageing process resulting in logarithmic loss of Capacitance

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Introduction

Capacitor ageing (Capacitance Drift) is a term used to describe the negative, logarithmic capacitance change that takes place in ceramic capacitors with time. The ageing process has a negligible affect on Class 1 (C0G) product but should be taken into account when measuring Class 2 (X7R, Y5V & Z5U) product.

The crystalline structure for Barium Titanate based ceramics changes on passing through its Curie temperature (known as the Curie Point) at approximately 125°C. The domain structure relaxes with time and in doing so, the dielectric constant reduces logarithmically, this is known as the ageing mechanism of the dielectric constant. The more stable dielectrics have the lowest ageing rates.

The start point for the ageing process is indicated for all product supplied by Syfer by the date stated on the packaging labels. If the ageing start point is not known then the ageing process can be reset by heating the capacitors to a temperature above the Curie Point. The ageing process then starts again from zero.

Law of Capacitance Ageing

During the first hour after cooling through the Curie temperature, the loss of capacitance is not well defined, but after this time it follows a logarithmic law that can be expressed in terms of an ageing constant.

The ageing constant '*k*', or ageing rate, is defined as the percentage loss of capacitance due to the ageing process of the dielectric that occurs during a decade of time (a tenfold increase in age) and is expressed as percent per logarithmic decade of hours. As the law of decrease of capacitance is logarithmic, this means that in a capacitor with an ageing rate of 1% per decade of time, the capacitance will decrease at a rate of:

i) 1% between 1 and 10 hours

ii) an additional 1% between the following 10 and 100 hours

iii) an additional 1% between the following 100 and 1,000 hours

iv) an additional 1% between the following 1,000 and 10,000 hours etc.

The ageing rate continues in this manner throughout the capacitors life.

An alternative method of expressing this is that the percentage loss of capacitance will be 2 times '*k*' between 1 and 100 hours and 3 times '*k*' between 1 and 1,000 hours. This may be expressed mathematically by the following equation:

$$C_t = C_1 \left[1 - \frac{k}{100} \log_{10} t \right]$$

Where: C_t is the capacitance t hours after the start of the ageing process

C_1 is the capacitance 1 hour after the start of the ageing process

k is the ageing constant in percent per decade (as defined above)

t is the time in hours from the start of the ageing process

The ageing constant may be declared by the manufacturer for a particular ceramic dielectric, or it may be determined by de-ageing the capacitor and measuring the capacitance at two known times thereafter.

Typical values of the ageing constant for Syfer Technology ceramic capacitors are:

Dielectric Class	**Typical Value**
C0G (CG/1B)	Negligible
X7R (2C1)	1% per decade

Example of a different dielectric material/ type offered by other capacitor manufacturers:

Dielectric Class	**Typical Value**
Z5U (2F4)	6% per decade

Capacitance Measurements

Ageing Allowances

Because of ageing, it is necessary to specify an age for reference measurements at which the capacitance shall be within the prescribed tolerance. This is fixed at 1,000 hours, since for practical purposes there is not much further loss of capacitance after this time.

In order to calculate the capacitance C_{1000} after 1,000 hours the following formula may be used:

$$C_{1000} = C_t \left[1 - \frac{k}{100} \left(3 - \log_{10} t \right) \right]$$

For measurements during the course of capacitor manufacture, the loss of capacitance from the time of measurement to the 1,000 hour age will be known and can be off-set by using asymmetric inspection tolerances. For example, if it is known that the total capacitance loss to 1,000 hours will be 5%, then the capacitors may be inspected to limits of say -15%/+25% instead of ± 20%.

All capacitors shipped are within their specified tolerance at the standard reference age of 1,000 hours after cooling through their Curie temperature.

Ageing begins after cooling from above the Curie point and continues, apparently forever. This capacitance loss does not limit the effective life of the capacitor, however, it should not be overlooked. A 1% change of capacitance value between 1 and 10 hours may seem serious but 1% change between 10,000 and 100,000 hours is less significant.

Refer to Appendix 1 showing the tolerance correction (for standard reference age of 1,000 hours) to allow for ageing rates of 1% and 6% between 12 and 10,000 hours.

Ageing Allowance Example

A capacitor with a tolerance of ± 20% is measured after 3750 hours from its last heat cycle. The corrected tolerance limits to which it should be tested are:

a) For 1% ageing; tolerance correction is: -0.6%

Therefore, tolerance range allowed is: -20.6% to +19.4%

b) For 6% ageing; tolerance correction is: -3.4%

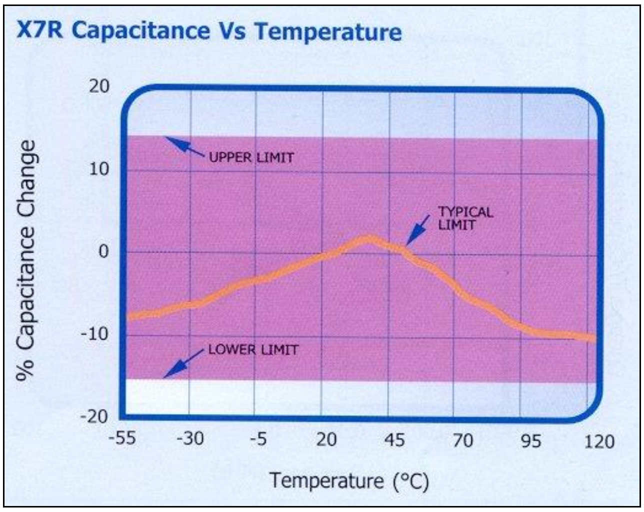
Therefore, tolerance range allowed is: -23.4% to +16.6%

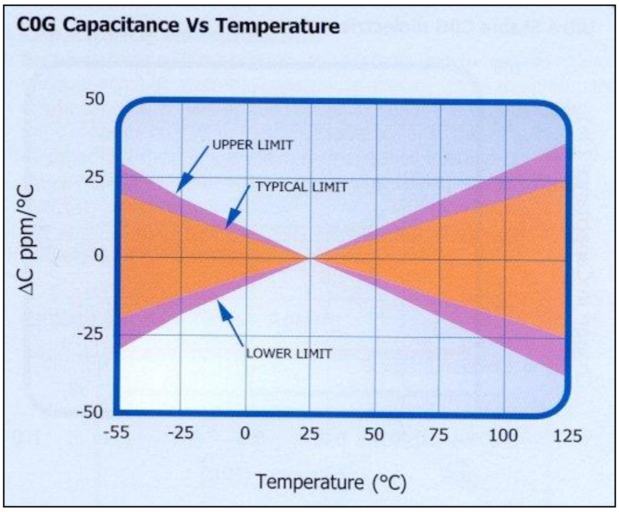
Test Temperature

Capacitance is normally declared at a reference temperature, this varies according to specification dependent on country of origin, for example CECC specifies 20˚C ± 2°C.

Capacitors measured at Syfer are tested in accordance with CECC specifications at 20°C. If capacitors are tested at a different temperature then allowances should be made when verifying the capacitance value.

Care should be taken when testing capacitors. Errors can arise if capacitors are heated by body heat through handling and it is recommended that for precision measurement plastic tweezers be used to handle capacitors.





Test Frequency and Voltage

The following table details the frequency and voltage settings used for electrical testing of surface mount and radial product types by dielectric classification.

Dielectric Class	Surface Mount		Radial product	
	Test Frequency	Test Voltage (rms)	Test Frequency	Test Voltage (rms)
C0G (CG/1B)	≥1nF = 1kHz <1nF = 1MHz	1.0V	1kHz	1.0V
X7R (2C1)	1kHz	>25V = 1.0V ≤25V = 0.5V	1kHz	0.5V

Measuring Equipment and Measurement Uncertainties

Incorrect capacitance measurement can also be introduced as a result of either the accuracy of the equipment and/ or measurement uncertainties.

- Measuring equipment. The accuracy and precision of the measuring device/ meter should be examined to determine if the meter is capable of measuring the capacitor adequately.
- Measurement uncertainties. Errors should be removed before measuring the capacitors. For example, by performing open and short-circuit compensations.
- Low capacitance measurements can be affected by stray capacitance from equipment test leads. It is recommended that when measuring values less than 50pF test fixtures are used to minimise the possibility of stray capacitance.
- As a result of the piezoelectric nature of ceramic capacitors, tweezer pressure can also affect capacitance measurements.
- Low capacitance radial products can also be affected by stray capacitance from the components legs/ leads. It is recommended that radial products are measured across the leads directly next to the component body.

Resetting the Ageing Process

For Class 1 (C0G) ceramics the ageing rate is negligible. For Class 2 ceramics it may be necessary to reset the ageing process.

The ageing process is reset by heating the dielectric above its Curie Point. To ensure that all capacitors have been sufficiently heated and that the ageing process has been reset it recommended that capacitors are placed in an oven @ 160°C for 1½ hours separated on a metal tray. After the heating process, the capacitors should then be allowed to stabilise at room temperature (20°C ± 2°C) for 24 hours before capacitance measurements are conducted.

Capacitance Tolerance & Circuit Application

Capacitance ageing is inherent in class 2 ceramic capacitors and it is important for circuit designs to recognise and allow for this effect. It is of particular importance when initial capacitance tolerance must be tight. In these circumstances the ageing rate may cause the capacitors to drift out of tolerance on the low side. For example, it would be imprudent to specify a 5% tolerance for a unit with a 2% ageing rate.

Designing the capacitor with an initial value large enough to compensate for long term ageing will cause the units to be out of tolerance on the high side each time de-ageing occurs. This can be especially true for equipment where an ambient operating temperature of +125°C could cause potential de-ageing. For this reason tight tolerance capacitors should be of class 1 dielectric when possible.

Summary & Conclusions

1. Electrical Tests. The recommended sequence for testing Multilayer Ceramic Capacitors is:
   - i) Insulation Resistance (IR)
   - ii) Voltage Proof (VP)/ Dielectric Withstand Voltage (DWV)
   - iii) De-age Class 2 capacitors and allow to stabilise at room temperature for 24 hours before capacitance measurements are conducted.
   - iv) Capacitance, apply factors based on the manufacturers ageing rate and the time elapsed since the last Curie temperature excursion.
   - v) Dissipation Factor.
   - vi) Other Tests. If any limits are specified for change in capacitance during a long term test, the capacitor should be de-aged before both the initial and final measurements.
2. With surface mount MLC's some of the solder termination materials used will diffusion bond at temperatures close to that of the ceramic Curie temperature. It is, therefore, important that when de-ageing these products they should be placed on a tray such that their termination end surfaces are not in contact with each other.
3. The ageing process is completely repeatable and predictable for a given capacitor.
4. Capacitance change is negative and logarithmic in respect to time.
5. Application of a D.C. bias can move the point on the ageing curve forward in time. When a D.C. voltage is applied at elevated temperatures (below the Curie Point) the capacitor will show a loss of capacitance but with a consequently lower ageing rate.
6. Class 1 CG/1B (C0G) dielectric has a negligible ageing rate.
7. Class 2 ceramic dielectrics have ageing rates which may vary from 0.6% to 8%. Dependent upon particular ceramic composition employed, this wide capacitance change, as a result of

'Shelf' ageing and temperature cycling, illustrates why tight-tolerance (less than ± 5%) high dielectric constant ceramics should only be specified with caution.

8. Soldering both leaded and surface mount class 2 capacitors into a circuit will, because of the ageing phenomenon, give an increase in capacitance as a result of the soldering temperature being greater than the dielectric Curie Point. The magnitude of the change will be dependent on the soldering temperature, time and the dielectric class.

Appendix 1 Tolerance Correction For Ageing Rates of 1% and 6%

For Standard Reference Age Of 1,000 Hours

Hours Since Last Heat Cycle	1%	6%	Hours Since Last Heat Cycle	1%	6%
12	1.9	11.5	1000	0.0	0.0
14	1.9	11.1	1050	0.0	-0.1
16	1.8	10.8	1100	0.0	-0.2
18	1.7	10.5	1150	-0.1	-0.4
20	1.7	10.2	1200	-0.1	-0.5
22	1.7	9.9	1250	-0.1	-0.6
24	1.6	9.7	1300	-0.1	-0.7
26	1.6	9.5	1350	-0.1	-0.8
28	1.6	9.3	1400	-0.1	-0.9
30	1.5	9.1	1450	-0.2	-1.0
32	1.5	9.0	1500	-0.2	-1.1
34	1.5	8.8	1600	-0.2	-1.2
36	1.4	8.7	1700	-0.2	-1.4
38	1.4	8.5	1800	-0.3	-1.5
40	1.4	8.4	1900	-0.3	-1.7
45	1.3	8.1	2000	-0.3	-1.8
50	1.3	7.8	2100	-0.3	-1.9
55	1.3	7.6	2200	-0.3	-2.1
60	1.2	7.3	2300	-0.4	-2.2
65	1.2	7.1	2400	-0.4	-2.3
70	1.2	6.9	2500	-0.4	-2.4
80	1.1	6.6	2600	-0.4	-2.5
90	1.0	6.3	2700	-0.4	-2.6
100	1.0	6.0	2800	-0.4	-2.7
120	0.9	5.5	2900	-0.5	-2.8
140	0.9	5.1	3000	-0.5	-2.9
150	0.8	4.9	3250	-0.5	-3.1
175	0.8	4.5	3500	-0.5	-3.3
200	0.7	4.2	3750	-0.6	-3.4
225	0.6	3.9	4000	-0.6	-3.6
250	0.6	3.6	4250	-0.6	-3.8
275	0.6	3.4	4500	-0.7	-3.9
300	0.5	3.1	4750	-0.7	-4.1
350	0.5	2.7	5000	-0.7	-4.2
400	0.4	2.4	5250	-0.7	-4.3
450	0.3	2.1	5500	-0.7	-4.4
500	0.3	1.8	5750	-0.8	-4.6
550	0.3	1.6	6000	-0.8	-4.7
600	0.2	1.3	6500	-0.8	-4.9
650	0.2	1.1	7000	-0.8	-5.1
700	0.2	0.9	7500	-0.9	-5.3
750	0.1	0.7	8000	-0.9	-5.4
800	0.1	0.6	8500	-0.9	-5.6
900	0.0	0.3	9000	-1.0	-5.7