Capacitor Ratings

Exceeding the maximum recommended stress levels on a ceramic multilayer capacitor can reduce the useful life of the capacitor or lead to catastrophic failure. The maximum stress levels effecting capacitor reliability are a function of the safe maximum current carrying capacity as manifested by excessive voltage potential appearing across the capacitor or by excessive temperature rise within the capacitor.

Voltage Effects:

Excessive voltage can cause failure either by damaging the dielectric insulating material between the capacitor plates or by causing arcing over the surface of the capacitor between the end terminations.

Voltage levels sufficient to support the external breakdown phenomenon are dependent on RF frequency, pressure [altitude], dirt, moisture, or other contaminants [solder flux] on the surface of the capacitor and by contaminants between the capacitor and the printed wiring board. Note also that circuit trace [mounting pad] spacing, generally closer than the MLC terminations, can contribute to arcing at values substantially lower than rated capacitor voltages. For guidance in developing printed wiring DLI recommends referencing industry standards.

The dielectric withstanding voltage, DWV is the maximum voltage rating for the capacitor and is based on the ultimate ability of the dielectric to resist damage from high field intensities.

The working voltage, i.e. WVDC, is the maximum continuous voltage that the capacitor is designed to handle. Exceeding this value will impact the reliability of the capacitor and reduce the useful life. The peak RF voltage plus any dc voltage on the capacitor should not exceed this value. The WVDC is established as a percentage of the DWV.

Thermal Effects:

The temperature rise within the capacitor must not exceed recommended values. Excessive temperature rise can damage the capacitor and potentially melt solder connections. Excessive temperatures in any electronic component can impact the long term reliability of that component. The maximum continuous operating temperature for ceramic multilayer capacitors is recommended to be no more than +125 ^{o}C.

The temperature rise will be a function of the amount of heat generated within the capacitor and the ability of the adjacent circuitry and structure to remove the heat. The power dissipated within the capacitor is a function of the RF current and the equivalent series resistance, esr. The esr quantifies all the loss mechanisms in the capacitor and constitutes the heat source. The rate of energy transfer, Q [Joules/second or Watts], from the heat source to the heat sink will depend on the physical dimensions of the heat path [Area and Length], the temperature gradient [ΔT] , and the thermal conductivity [k in Watts/meter – degree Kelvin] of the materials in the heat path.

$Q = (A/L) \times k \times \Delta T$ [J/sec or W]

Predicting the thermal performance of the capacitor is difficult due to the complexity of the heat path and the variety of printed wire board materials in use today. The heat path consists of the component attach material – solder or epoxy, the circuit conductor trace of gold or copper [width and thickness], the substrate material [alumina, FR-4, or others], and the proximity of other heat generating components such as transistors, resistors, etc. Note that inductors often used in conjunction with capacitors and mounted in close proximity have Q's significantly lower than DLI multilayer capacitors and can be a major heat source.

Actual in-circuit measurement of the thermal performance of a component or finite-element thermal analysis is recommended during the design process.

SJR   23 February 2011

Example:

This example invokes many simplifying assumptions. A single, continuous wave [CW] excitation is assumed. When considering a complex waveform, all the Fourier components need to be considered. Harmonic energy must be included. The circuit is assumed to be matched and addresses incident energy only.

Quantify the heat path from the heat source to the heat sink. A single thread path is defined as the thermal resistance of the capacitor to the substrate, θ_{JS}, and the thermal resistance of the substrate to the heat sink, θ_{SH}. Θ_T is the sum of these values. For the example Θ_T is set at 20 ^{o}C/W; a value that might be observed in a circuit implemented in alumina. Note that circuitry implemented on "soft" substrate materials, i.e. composites of glass fiber, epoxy, PTFE, ceramic, etc. in some combination will have a significantly poorer thermal conductivity. Subsequently, the current carrying capability of components mounted on these materials will be less due to the resultant higher thermal resistance.

Select the frequency for analysis: 250 MHz.

For a C17CF470 capacitor [47 pF] select the esr for the subject capacitor from the DLI data sheet, i.e. 0.032 Ω at 150 MHz. If the frequency of interest is different than the esr measurement frequency recalculate using the relationship:

$$\text{esr @ fb} = \text{esr @ fa} \times \sqrt{\frac{f_b}{f_a}}. \quad \text{Thus the esr @ 250 MHz} = 0.032 \times \sqrt{\frac{250}{150}} = 0.0413 \ \Omega.$$

Assume the heat sink temperature value is +85 ^{o}C. Determine power dissipation required to raise the temperature from this value to +125 ^{o}C - a rise of 40 degrees. The power required to product this temperature increase is the temperature rise divided by the thermal resistance:

$$P = 40 \ ^o\text{C} / \Theta_T = 40 \ ^o\text{C} / 20 \ ^o\text{C/W} = 2 \ \text{Watts}$$

Compute the rms value of current required to generate this level of power.

$$\text{Irms} = \sqrt{\frac{\text{power}}{\text{esr}}} = \sqrt{\frac{2 \cdot W}{0.0413 \cdot \Omega}} = 6.96 \ \text{Amps}_{rms}$$

Verify that the operating voltage across the capacitor does not exceed the maximum recommended working voltage $V_p = \sqrt{2} \times 6.96 \times (1/\omega C)$ or $V_p = \sqrt{2} \times 6.96 \times 1/(2 \times \pi \times 250 \text{ MHz} \times 47 \text{ pF}) + \text{dc voltage}$ [the dc voltage is assumed to be 0 volts in this example]. The peak voltage, V_p, of 133.3 Volts is well within the rating of the capacitor.

Comment:

To insure maximum component reliability a recommended practice is to follow the military guidelines and derate current and voltage to 50 to 60% of the rated values.

DLI C11 Multilayer Capacitors
0.055 x 0.055 inch

Current (Amps rms) vs Capacitance (pF)

Legend:
- C11AH
- C11CF
- C11UL

Working Voltage Spec Transition

AH & CF

@ 150 MHz
Thermal Resistance ~ 40 °C/W
Assumed temperature rise: 40 °C

DLI C17 Multilayer Capacitors
0.110 x 0.110 inch

Current (Amps rms) vs Capacitance (pF)

Legend:
- C17AH
- C17CF
- C17UL

@ 150 MHz
Thermal Resistance ~ 20 °C/W
Assumed temperature rise: 40 °C

DLI C22 and C40 Multilayer Capacitors
0.220 x 0.245 inch and 0.380 x 0.380 inch

C22AH
C40AH

@ 150 MHz
C22's - Thermal Resistance ~ 15 ºC/W
Assumed temperature rise: 40 ºC

@ 15 MHz
C40's - Thermal Resistance ~ 12 ºC/W
Assumed temperature rise: 40 ºC

Current (Amps rms)

Capacitance (pF)