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Micro sectioning Of Multilayer Ceramic Capacitors

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Introduction

Preparation of Multilayer Ceramic Capacitors micro sections involves the use of techniques which can create artifacts, which in turn can be misinterpreted as capacitor faults. The purpose of this document is to provide a guide to preparation and examination of micro sections, so that results reflect the true internal properties of the parts being examined.

It is recommended that fracture sections examined using a Scanning Electron Microscope are used in conjunction with micro sectioning, in order to gain the most information. This technique is also detailed within this document.

Potting of Components

Components are normally applied to a double sided sticky tape, in the orientation appropriate for examination. Components should be separated from one another by a reasonable gap to allow potting compound to surround each component. If components are too close, they can be poorly supported by resin, and can be damaged around the chip edges during grinding.

A suitable sized mould should be used to contain the components, so that each component is a reasonable distance from the edge of section stub.

Choice of potting compound is very important. Use of a low price general purpose resin will almost certainly generate damage around the chip edges during grinding. Consequently use of a high quality, low stress potting compound is recommended.

Grinding of Micro Section

Waterproof Silicon Carbide grinding paper is available in many grit sizes. Paper should be selected as appropriate to the sample being prepared, and the degree of finish required for examination of the finished section. In cases where the best quality micro section is required, it is recommended that nothing coarser than 800 grit paper is used, with 1200 grit or finer being used prior to final polishing.

Direction of grinding is important, and can influence the results generated. Syfer has determined that in most cases, multi directional grinding gives the best results.

It is possible to determine in some cases whether faults are real or artifacts by changing the grinding direction periodically, and examining the micro section at each stage.

Polishing of Micro Section

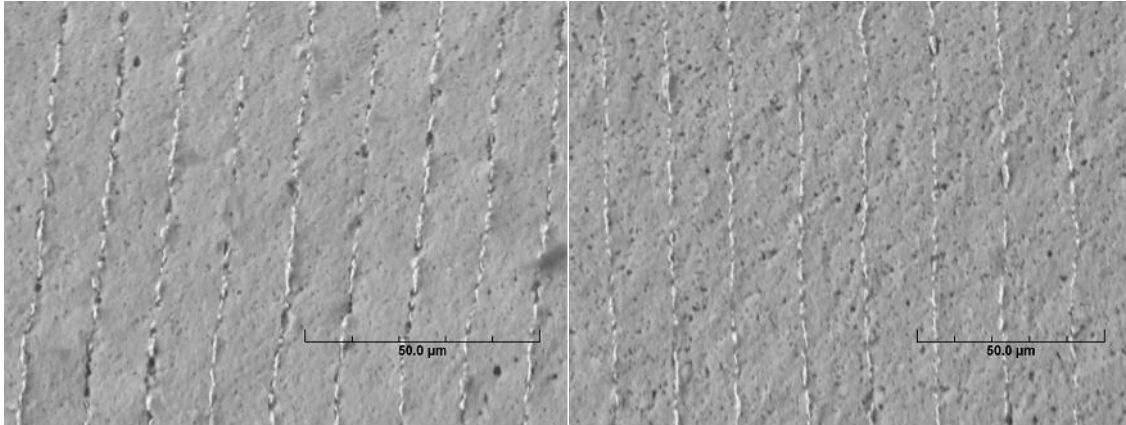
It is common to use fine diamond slurries to polish micro sections. These may be of very fine particle size (example 0.1 micron), but they have been found to create damage to Multilayer Ceramic Capacitors, as the diamond is harder than the ceramic material being polished.

Syfer recommend the use of an alumina based polish, which does not create any damage to the parts being polished. Syfer use a fine alumina powder, which is made into a slurry using deionised water.

As with grinding, polishing should be multi directional.

Fracture Sections

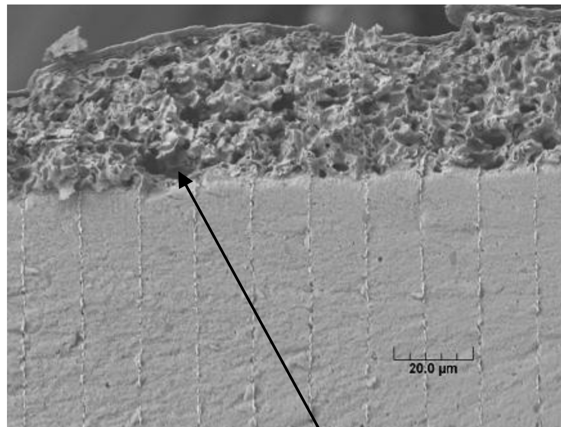
Fracture sections are obtained by breaking a chip so that the internal electrodes are exposed. Ease of fracturing is highly dependent on the physical dimensions of the part to be fractured. In order to make a good fracture section, it is important to break the chip without applying too much pressure. It may help to scribe the chip at the point where the fracture is required prior to applying pressure. Fractured edges should be examined optically prior to using the SEM, and only the best fractures used for detailed analysis.



Fracture Section
X7R 1 – High density material

Fracture Section
X7R 2 – Lower density material

Unfortunately, fracture sections are generally unsuitable for looking at chip / termination / plating boundaries, as there are definite stresses applied to the termination interfaces during fracturing, and the edges of the termination bands are particularly vulnerable.



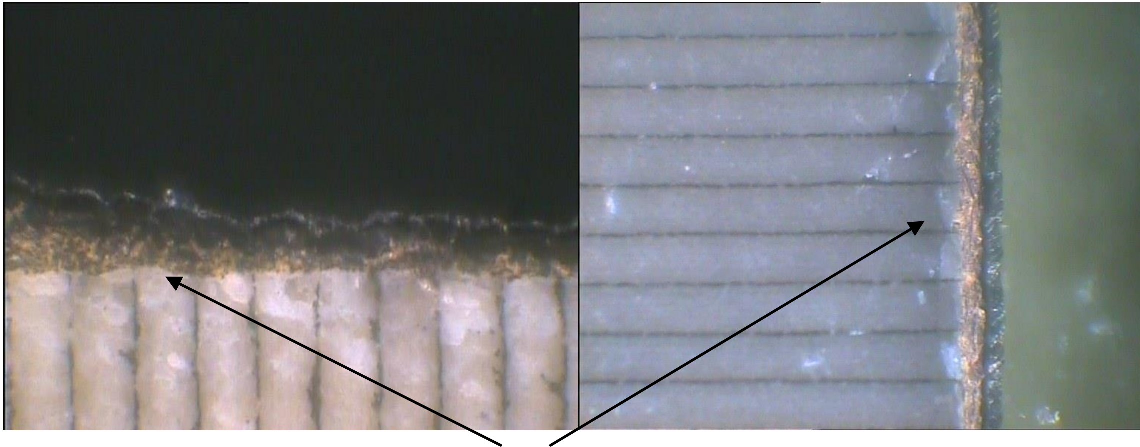
Fracture section showing some damage at termination boundary

Examples of Sectioning Artifacts

A. Termination / Chip Interface Cracking

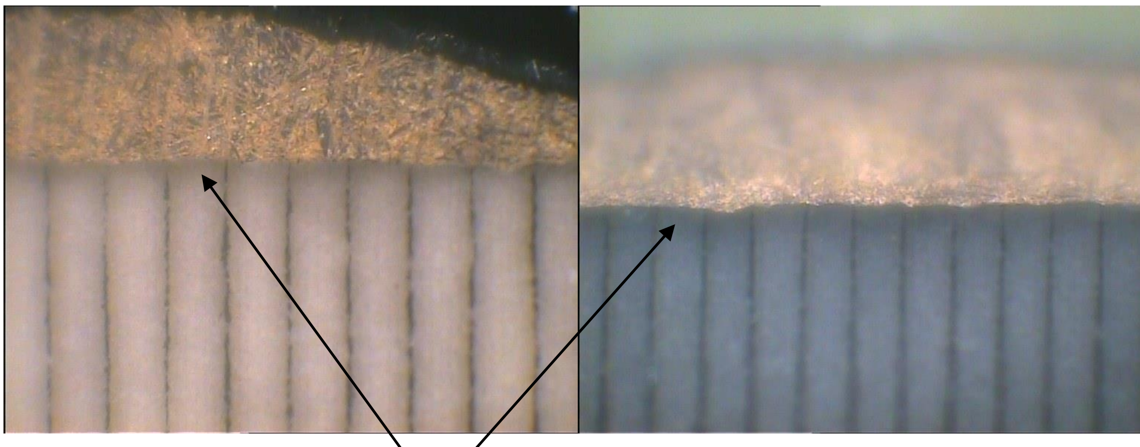
This is an example of an artifact that may be present particularly when grinding along the electrodes, and less evident when grinding perpendicular to the electrodes.

Stress relief between the ceramic chip and the termination can take place during grinding. This is most common where the relative hardness of the ceramic and termination materials are different, such as in the Syfer 'Flexicap' range of parts, which uses a polymeric termination primarily to reduce mechanical cracking issues.



Cracks at termination / chip interface caused by stress relief due to unsuitable grinding

Using a refined sectioning technique, and grinding perpendicular to the electrodes, it was possible to eliminate the cracks, confirming them as artifacts.



No cracks evident at termination / chip interface on correctly ground specimen

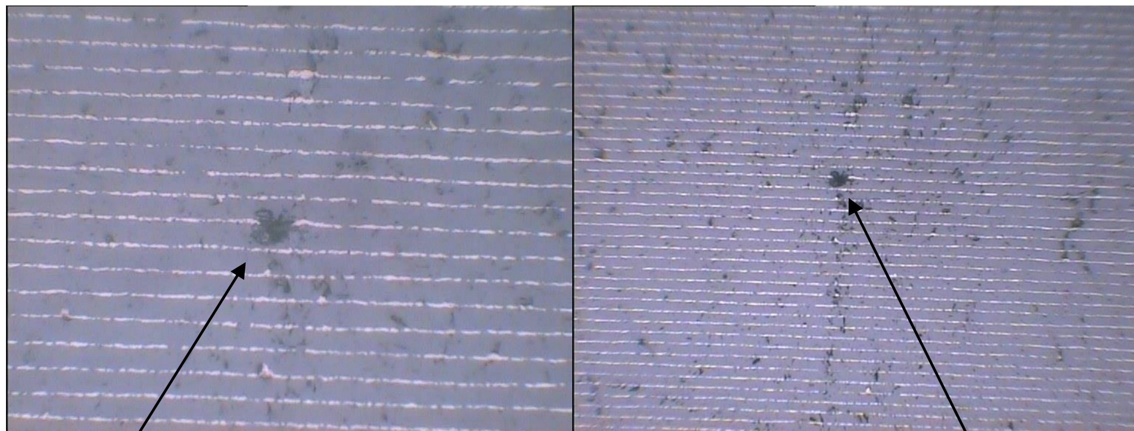
B. Voids Within the Dielectric Structure

Ceramic materials as used to manufacture Multilayer Ceramic Capacitors vary greatly in fired structure. Some materials produce a denser structure than others after fire, and grain size can vary significantly.

This means that ceramic materials can behave differently when micro sectioned and some materials can be more prone to pull out of the fired structure than others.

Pull out occurs when the ceramic structure is damaged by the grinding process, causing a fragment of the ceramic to be removed, leaving a void. When examined

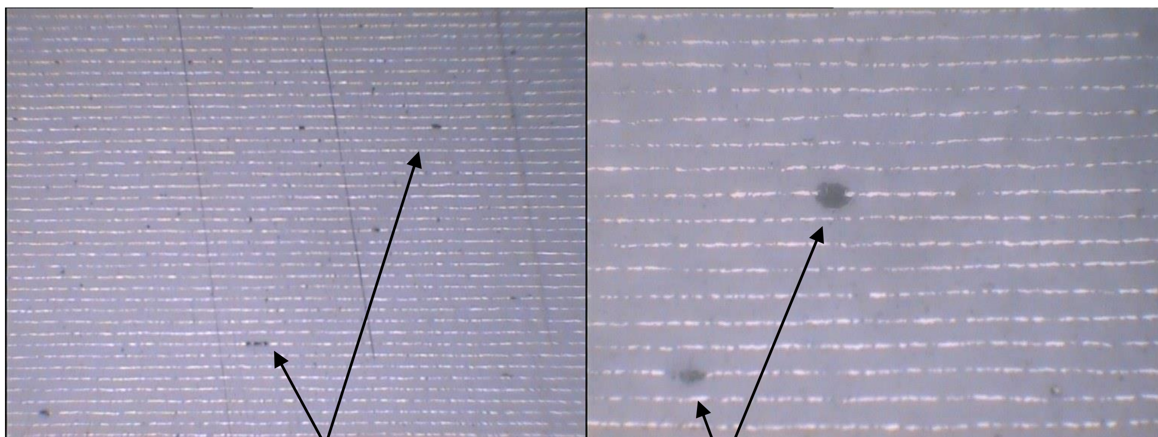
prior to polishing it is common to see lines of pull out following the scratch marks on a section.



Void within dielectric structure

The same void, seen as pullout Formed as part of a scratch

Depending on grinding media and technique used, it is possible to damage the ceramic to a significant depth below the surface, meaning that the damage can still be apparent after careful fine grinding and polishing.



Polished sections, showing voids due to pullout

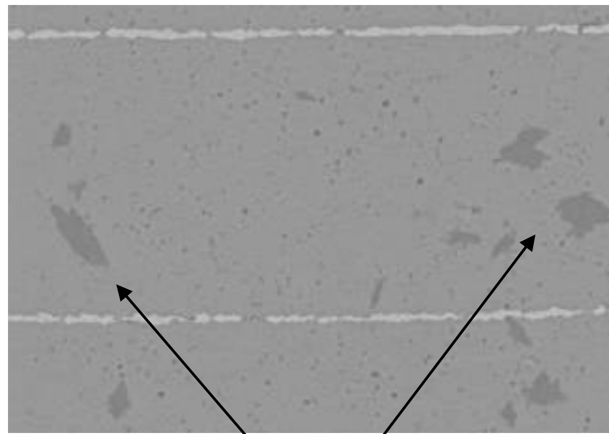
In general, a genuine void will almost always be accompanied by some form of distortion of the layers nearest to the void, and as such, is straightforward to identify as a true fault.

Structural Abnormalities

It is relatively common to find ceramic 'dendrites', 'inclusions' or areas of a 'second phase' within the general ceramic structure of multilayer ceramic capacitors. These areas are most apparent when viewed under a Scanning Electron Microscope, particularly when using a backscatter detector, but they can also be visible under an optical microscope fitted with a polarizing filter.

Structural abnormalities generally take the form of irregularly shaped microstructures within a bulk ceramic microstructure. The existence of these areas is not uncommon in many compositions. For X7R materials, which are practically all barium titanate based, the 'dendrite' is usually a titania rich area, relative to the bulk material. The exact

composition may vary due to influences from the electrode material (which itself may be doped with a ceramic material as a shrinkage aid), but will also be present in the insulation layers and margins.



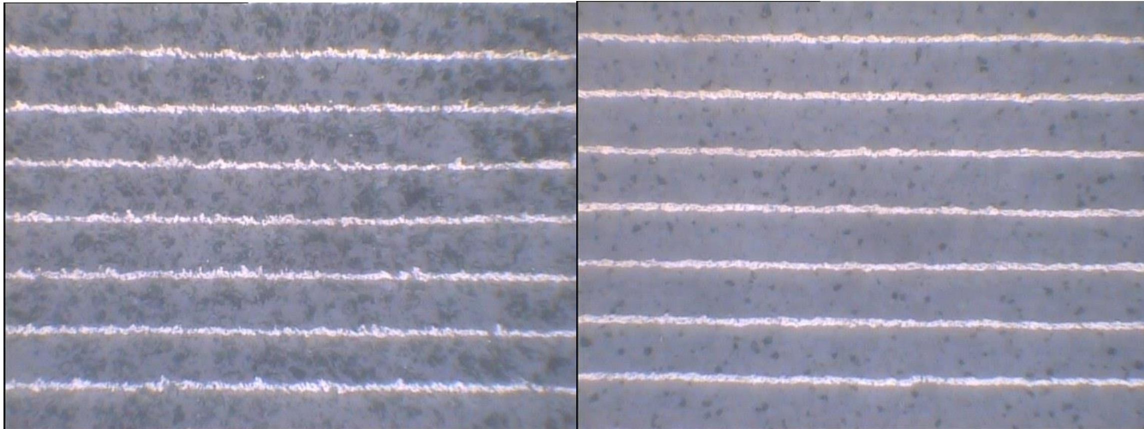
Examples of 'dendrites'
in X7R

Where present, these structural abnormalities do not affect electrical performance of the components in any way. Product reliability is also unaffected.

Depending on their exact composition, structural abnormalities may be of a slightly different density (typically higher density) than the general ceramic structure. This density difference makes the abnormal areas more susceptible to pull out during micro sectioning, often resulting in the misdiagnosis of a void.

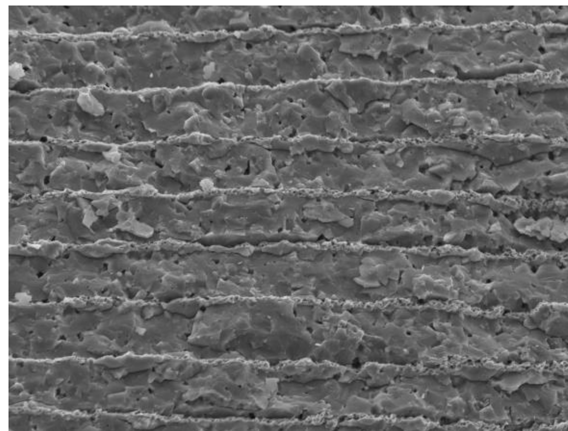
Ceramic Grain Size

Some dielectric materials (particularly COG) may have a large fired grain size. These materials are especially difficult to micro section, as they virtually impossible to grind and polish without causing pullout of grains, which being relatively large, will always appear as voids within the dielectric structure. These materials require extra fine grinding and careful polishing when preparing sections and it is particularly recommended that fracture sections are used to verify structure.



Large grained material
Poorly prepared section

Large grained material
Good quality section



Large grained material
Fracture Section SEM Image