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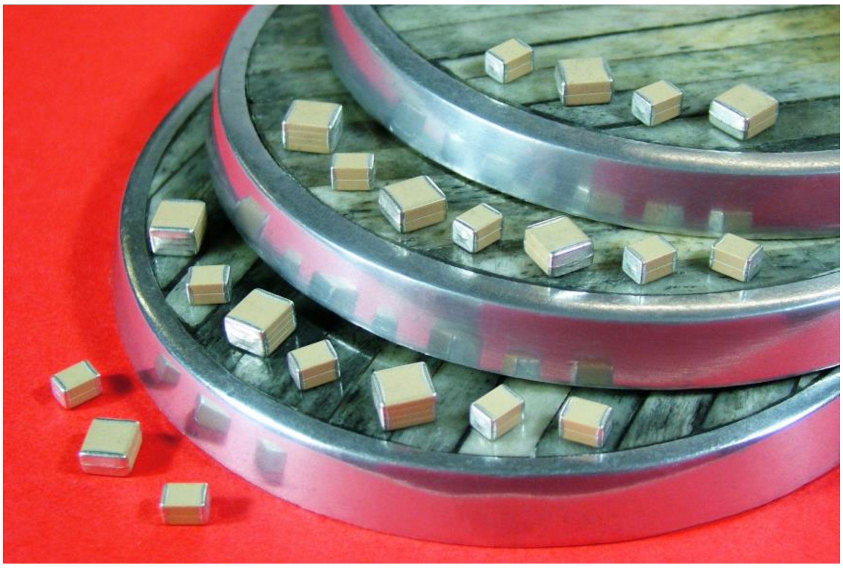
# StackiCap™ High Voltage High CV MLCC

## Introduction



Syfer StackiCap™ surface mount MLCs are designed to provide high CV in compact packages and offer the greatest volumetric efficiency and CV per unit mass of any high voltage X7R ceramic capacitors available. Syfer has conceived, developed and protected, GB Pat. App. 1210261.2, a unique process in order to deliver this groundbreaking product. Combined with FlexiCap™ stress relieving terminations these parts have the potential to replace film and tantalum capacitors and make many stacked products obsolete. StackiCap™ are suitable for a plethora of applications such as switch mode power supplies for filtering, tank and snubber, DC-DC converter, DC block, voltage multipliers etc. and will provide huge benefits in applications where size and weight is critical. At this moment 1812,2220 and 3640 case sizes have been launched and are commercially available, additional sizes up to 8060 are still under development, please see the Syfer website or contact the factory for the latest ranges.

## Downsizing Potential

Offering significant increases in available capacitance StackiCap™ can offer significant downsizing over existing technology, below are some images showing the benefits.

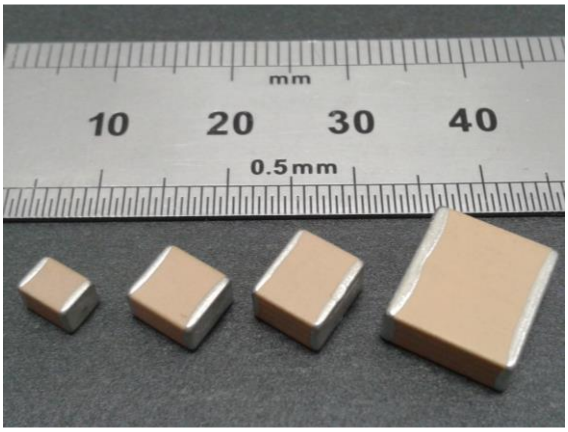



*Fig 1. StackiCap sizes 1812 to 3640*

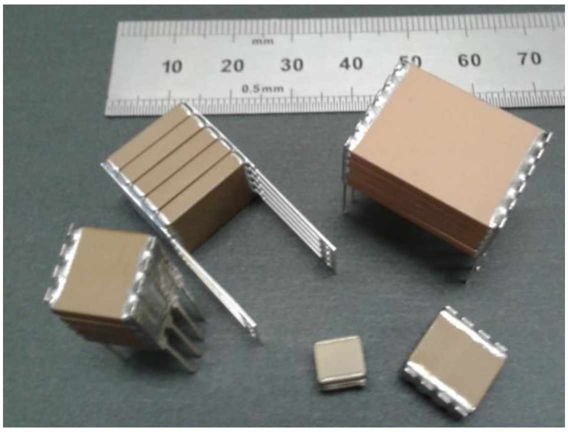



*Fig 2. Various stacked assemblies up to 8060 5 stack*

Figure 1 shows the initial StackiCap™ product range sizes of 1812, 2220, 2225 and 3640. 5550 and 8060 development sizes are not shown. Figure 2 shows a range of stacked and stacked leaded assemblies of sizes 2225, 3640, 5550 and 8060 up to a maximum of 5 in a stack. Figures 3 and 4 show examples of what can be replaced with a single StackiCap™ component. In the most extreme cases an 8060 1kV 470nF could be replaced with a single 2220 1kV 470nF and a 3640 1kV 180nF could be replaced with a single 1812 1kV 180nF, these are 10:1 and 7:1 footprint reductions respectively.

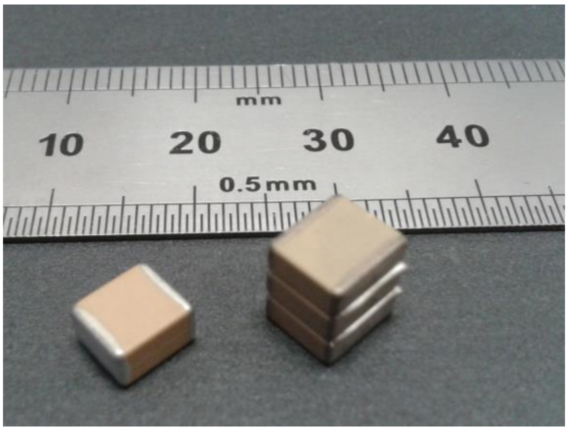



Fig 3. 2220 500V 1µF StackiCap™ & 2225 3 Stack 500V 1µF

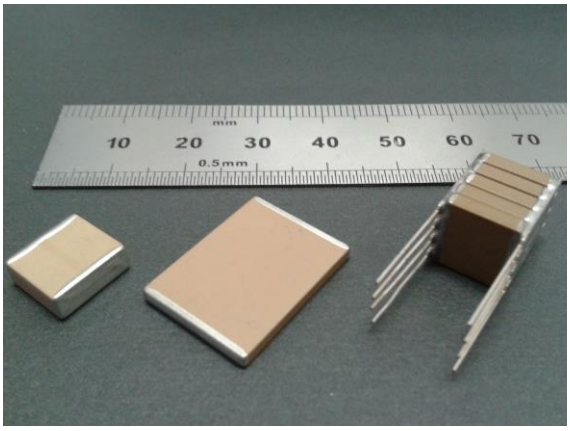



Fig 4. 3640 500V 3.3µF StackiCap with 8060 and 3640 5 stack alternatives

## Historical Limitations

The limits of design are defined by the failure modes and there are many failure modes which limit the extent to which mid to high voltage MLCC can be developed. There are extrinsic failure modes such as mechanical and thermal cracking but we will look at the intrinsic ones which are in the hands of the manufacturer. The limiting factor for MLCC has changed over time, early MLCC were limited mainly by the quality and purity of the dielectric materials themselves with point defects and contamination, fig 5, limiting the maximum number of layers and the minimum thickness of those layers. As dielectric materials and materials preparation and processing improved the limiting factor became the dielectric strength of the material itself. Once this point had been reached one could imagine that thicker and larger parts could be manufactured without fear of dielectric breakdown, fig 6, or point failures, however a new failure mode appeared, electro-mechanical stress cracking. Commonly referred to as piezo electric it can also follow electrostrictive behaviour, see fig 8. This is the failure mode that has been the limiting factor for MLCC manufactures for some time now, it affects most class II barium titanate base dielectrics and becomes an issue for larger size, 1210 upwards, and higher voltage, 200V upwards components. The crack typically runs through the centre of the component along one or two dielectric layers, fig 7. Most solutions involve stacking capacitors together with lead frames in order to increase the available capacitance for a given footprint but this is labour intensive, costly and can lead to other reliability issues.

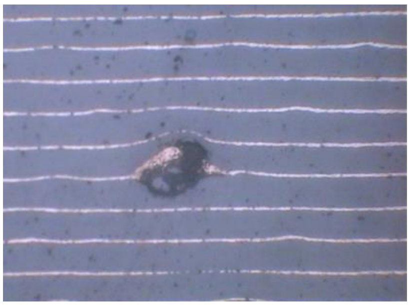


Fig 5. Contamination defect

Fig 6. Dielectric breakdown

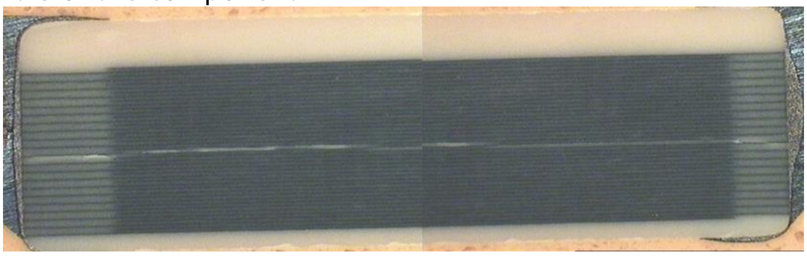


Fig 7. Piezo stress crack failure

Other solutions involve special dielectric formulations but these are usually a trade off for dielectic constant and therefore the ultimate capacitance value available.

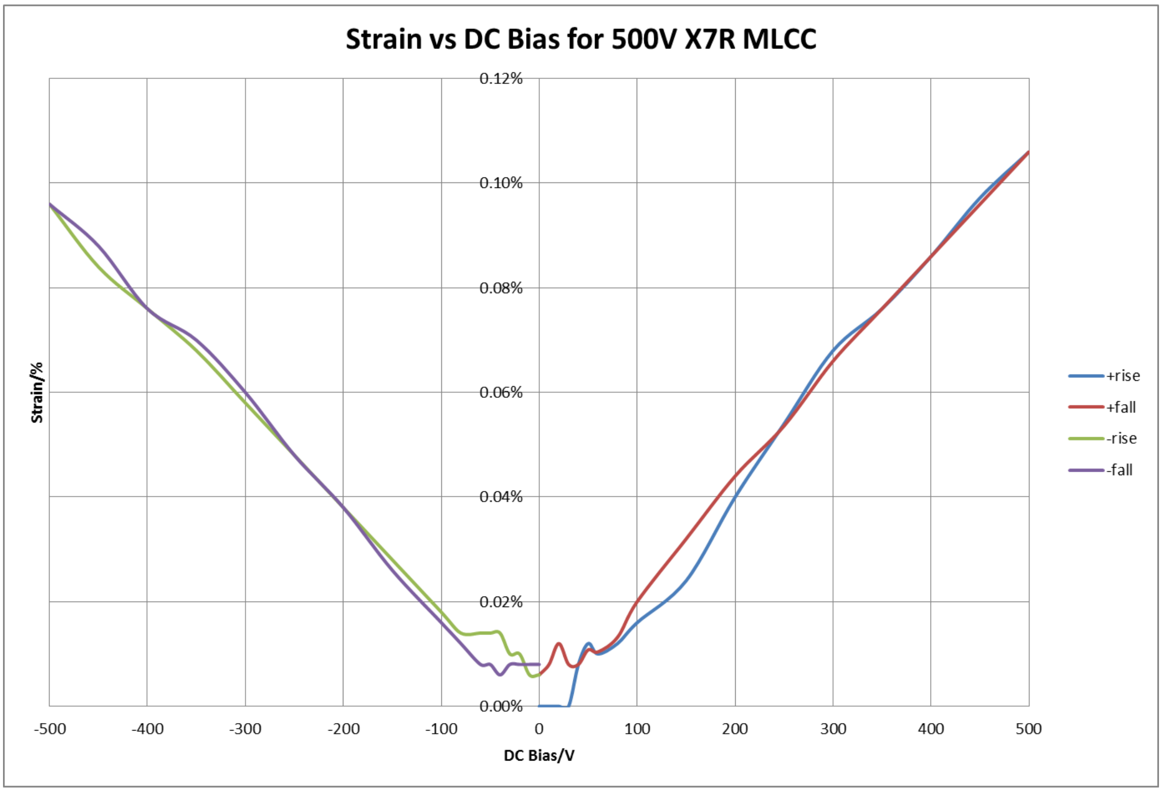



*Fig 8. An example of the mechanical response of an X7R MLCC under DC bias*

## The Technology Behind StackiCap™

After a series of trials and iterations Syfer have developed a single chip solution to electro-mechanical failure limitation, StackiCap™. The novel and patent pending aspect, GB Pat. App. 1210261.2, is an inbuilt stress relieving layer which allows the capacitor to exhibit the electrical and physical behaviour of multiple, thinner, components whilst exploiting the manufacture and process benefits of being a single unit. The stress relieving layer is made up of a combination of already utilised material systems and is formed during the standard manufacturing process. The layer is positioned in the place/s where mechanical stress is the greatest allowing for mechanical decoupling of the multiple component layers with 2,3 and 4 "stack"versions trialled at this point.With FlexiCap™ flexible termination material and no need to attach components together to form a stack there is no need for a lead frame allowing for standard tape and reel packaging with pick and place capability.

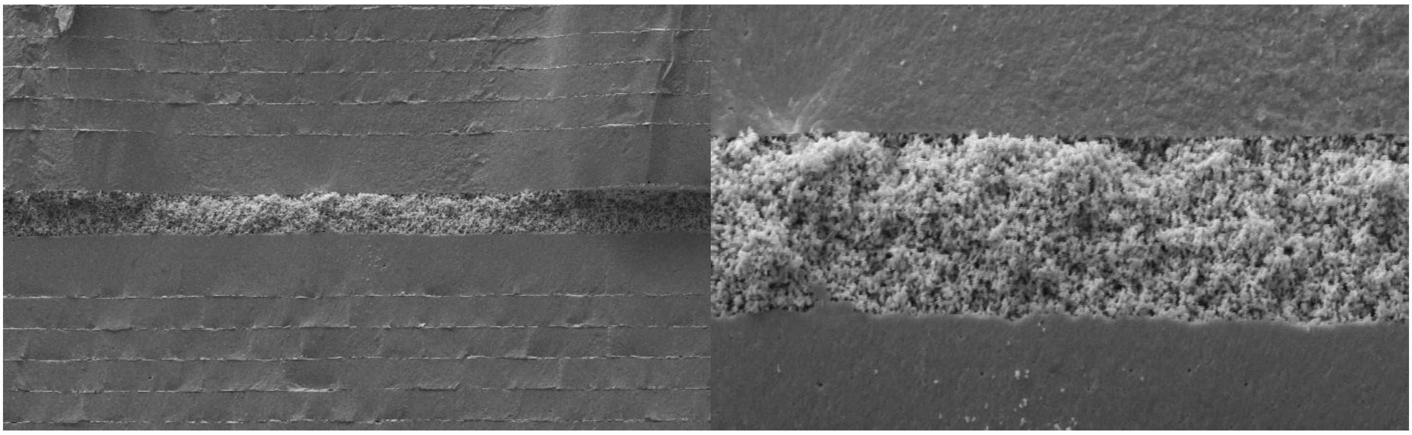


*Fig 9. SEM Micrograph of fracture sections showing the stress relieving "spongy" layer*

## Qualification Program

StackiCap™ technology has been under development at Syfer for some time, parts and materials have been subjected to Syfer's standard quality control and reliability regime, this is detailed below:

1. Material Verification (before use)

   All materials are inspected in accordance with defined specifications before being accepted for. For example, each new lot of dielectric powder is subjected to:

   - Powder size distribution analysis on milled ink.
   - Solids content and viscosity analysis of the subsequently manufactured ink.
   - Capacitor approval batch manufacture to perform:
   - Internal Destructive Physical Analysis examination.
   - Electrical tests for Capacitance, Dissipation Factor, Insulation Resistance and Dielectric Withstand Voltage.
   - Dielectric Constant measurement.
   - Endurance tests conducted at 125°C with 1.0 or 1.5x rated voltage applied.
   - TCC measurements
   - 85/85 tests.

2. Product Verification (during and after manufacture)

   As part of Syfer's standard production process each batch is subjected to a series of inspection and testing stages during which the quality of the product is examined and verified. These stages include:

   - Dielectric thickness measurements using lasers during the capacitor construction process.
   - Internal Destructive Physical Analysis. A sample of capacitors is taken from each batch and subjected to an internal visual examination to verify the capacitor construction.
   - Plating thickness measurements conducted using the X-Ray Fluorescence method.
   - Solderability and leach tests conducted by immersing capacitors into solder.
   - 100% production electrical tests for Capacitance, Dissipation Factor and Dielectric Withstand Voltage.

   These inspection and test stages are supported by:

   - Visual inspection stages conducted throughout the manufacturing process.
   - Statistical Process Control.
   - Final QC Inspection.

3. Routine Reliability Tests

   In addition to the standard inspection and tests performed during batch manufacture, a sample of batches is also randomly selected for additional routine endurance, humidity and bend tests.

   Reliability tests are also conducted by external test laboratories as part of maintaining product approvals and are also conducted at Syfer to assess long-term product performance.

   The reliability tests conducted at Syfer include:

   - Life Test. Capacitors are subjected to 1000 hours at 125°C with 1.0x or 1.5x rated voltage applied. The results of the Life Tests are used to calculate reliability Failure In Time (FIT) rate data. FIT rates are especially useful to customers because the data shows the capacitor product type reliability at the voltage and temperature being applied by the customer. The FIT rate data can be converted into other reliability units such as MTBF by using conversion factors.
   - 85/85. Capacitors are subjected to 168 hours at 85°C/ 85%RH.
   - Bend Tests. Capacitors are mounted on Syfer Test PCBs and subjected to bend tests to evaluate the mechanical performance of the components.

The released StackiCap™ range has passed all of the above testing and at the time of release of this document has amassed over 2000000 hours of reliability test time. Further testing is ongoing to ensure the highest levels of quality and reliability, please refer to the Syfer website for updated versions of this document and the latest range and quality information.

High Reliability testing is also ongoing with a full AEC-Q200 Rev D qualification under way for 1812 and 2220 case sizes details of the test program are below, additional rel qualification testing can be considered on request.

| Test ref. | Test | Reference | Sample Acceptance | | | Additional requirement |
|---|---|---|---|---|---|---|
| | | | P | n | C | |
| P1 | AEC-Q200 test 3. High Temp Storage | MIL-STD-202 method 108 | 12 | 77 | 0 | Unpowered 1000 hours @ 150°C. |
| P2 | AEC-Q200 test 4. Temperature cycling | JESD22 method JA-104 | 12 | 77 | 0 | 1000 cycles (-55°C to 125°C) |
| P3 | Moisture Resistance | MIL-STD-202 method 106 | 12 | 77 | 0 | t = 24 hours/cycle. Unpowered. |
| P4 | Biased Humidity | MIL-STD-202 method 103 | 12 | 77 | 0 | 1000 hrs 85°C/85%RH. 1.5 Vdc and Rated Voltage. |
| P5 | Operational Life | MIL-STD-202 method 108 | 12 | 77 | 0 | Rated Voltage @ 125°C. |
| P7 | Mechanical shock | MIL-STD-202 method 213 | 12 | 30 | 0 | Figure 1 of method 213 SMD: Condition F. |
| P8 | Vibration | MIL-STD-202 method 204 | 12 | 30 | 0 | 5 g's for 20 min., 12 cycles each of 3 orientations. Test from 10-2000Hz. |
| P9 | Resistance to Soldering Heat | MIL-STD-202 method 210 | 3 | 12 | 0 | Condition B No pre-heat of samples. |
| P11 | Adhesion, Rapid Temp Change & Climatic Sequence | BS EN 132100 | 12 | 27 | 0 | 5N force applied for 10s, -55°C/+125°C for 5 cycles, damp heat cycles |
| P12 | Board flex | AEC-Q200-005 | 12 | 30 | 0 | 3 mm deflection Class I ; 2 mm deflection Class II ; 1 mm deflection X7R (A,F,J) |
| P14 | Terminal strength | AEC-Q200-006 *CECC 32 101-801 group C3.1 | 12 | 30 | 0 | Force of 1.8kg for 60 seconds. *Force 0.5kg for 10 seconds for 0603 case size |
| P15 | Beam Load Test | AEC-Q200-003 | 12 | 30 | 0 | - |
| P16 | Damp Heat Steady State | BS EN 132100 4.14 | 12 | 45 | 0 | 56 days, 40°C/93%RH. 15x no volts, 15x5Vdc, 15xRv or 50v whichever is less |

# Range and Ordering Information

## Comparison chart - StackiCap™ capacitors

| Chip Size | Voltage | StackiCap™ range (nF) | Non- StackiCap™ range (nF) | Replaces Case Size |
|---|---|---|---|---|
| 1812 | 200/250V | 1000 | 680 | 2220 |
| | 500V | 470 | 330 | 2220 |
| | 630V | 330 | 180 | 2220 |
| | 1kV | 180 | 100 | 2225 / 3640 |
| | 1.2kV | 100 | 33 | 2225 |
| | 1.5kV | 56 | 22 | 2225 |
| 2220 | 200/250V | 2200 | 1000 | 3640 |
| | 500V | 1000 | 560 | 3640 |
| | 630V | 1000 | 330 | 5550 |
| | 1kV | 470 | 120 | 8060 |
| | 1.2kV | 220 | 82 | 5550 |
| | 1.5kV | 150 | 47 | 5550 |
| | 2kV | 100 | 27 | 8060 |
| 3640 | 200/250V | 5600 | 3300 | 5550 |
| | 500V | 2700 | 1000 | 8060 |
| | 630V | 2200 | 680 | 8060 |
| | 1kV | 1000 | 180 | 8060 |
| | 1.2kV | 470 | 150 | 8060 |
| | 1.5kV | 330 | 100 | 8060 |
| | 2kV | 150 | 47 | 8060 |

## Ordering information - StackiCap™ capacitors

| 1812 | Y | 500 | 0474 | J | X | T | WS2 |
|---|---|---|---|---|---|---|---|
| Chip size | Termination | Voltage | Capacitance in picofarads (pF) | Capacitance tolerance | Dielectric | Packaging | Suffix code |
| **1812**<br>**2220**<br>**3640** | **Y** = FlexiCap™ termination base with nickel barrier (100% matte tin plating). RoHS compliant. Lead free.<br>**H** = FlexiCap™ Termination base with nickel barrier (Tin/lead plating with minimum 10% lead). Not RoHS compliant. | **200/250** = 200/250V<br>**500** = 500V<br>**630** = 630V<br>**1K0** = 1kV<br>**1K2** = 1.2kV<br>**1K5** = 1.5kV<br>**2K0** = 2kV | First digit is 0. Second and third digits are significant figures of capacitance code in picofarads (pF). Fourth digit is number of zeros<br>eg. **0474** = 470nF<br>Values are E12 series | **J** = ±5%<br>**K** = ±10%<br>**M** = ±20% | **X** = X7R | **T** = 178mm (7”) reel<br>**R** = 330mm (13”) reel<br>**B** = Bulk pack - tubs or trays | **WS2** |

## Reeled quantities - StackiCap™ capacitors

| | 1812 | 2220 | 3640 |
|---|---|---|---|
| 178mm (7”) Reel | 500/1,000 | 500/1,000 | - |
| 330mm (13”) Reel | 2,000/4,000 | 2,000/4,000 | 500 |