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Presents

The "E-Field Choke"TM Application Note

GENERAL

Higher speed mixed signal semiconductor devices present different and more stringent requirements on decoupling elements and networks. The internal current switching transients developed in today's ICs can have pulse widths on the order of 200 to 1000 psec, generating significant noise signal components in what is generally considered microwave frequencies, 1 to 5 GHz. These noise components can be present on any or all input/output "pins" and they must be effectively dealt with to achieve the designer's expectations of wide dynamic range and system noise performance. A "low frequency" perspective which looks to solve decoupling requirements solely with current storage, bypass capacitors, may fall short of the actual circuit needs. No more can only the inclusion of a very large capacitor satisfy decoupling requirements. Instead, more sophisticated broad band decoupling and termination is required. A new class of decoupling circuit elements, the "E-Field Choke", is an appropriate device for these requirements.

The E-Field Choke is a monolithic device based on highly effective and reliable parallel plate ceramic capacitor technology. Instead of a uniform rectangular metalization defining the top plate of a capacitor, a specific pattern of conductor and resistor materials is defined on the top surface. This pattern was developed using microwave transmission line technology and tools to enhance shunt bypass capability and series attenuation while minimizing the always undesirable parasitic element resonance. In a simplified, DC and low frequency, model analysis the E-Field Choke can be viewed as a CRC network, see figure 1.

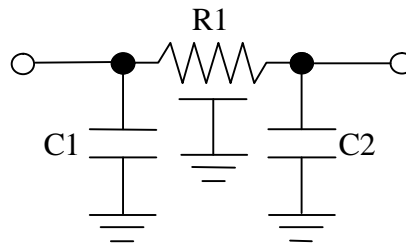


Figure 1

In a broader band model, though, there is an additional feature, higher attenuation with higher frequency or a lossy transmission line characteristic. It is this lossy transmission line which enhances decoupling performance. From microwave field theory, it is known that the current in micro strip transmission lines is concentrated along the boundaries in contact with the substrate and the edges in particular.

For the E-Field ChokeTM the edges of the effectively low impedance micro strip transmission line which crosses over the top surface of the capacitor is designed to have high loss. The result is that the higher frequency signals or noise components are attenuated at a much larger rate than with conductor-only patterns. Figures 2 and 3 compare the performance of an E-Field ChokeTM and a similar physical size parallel plate capacitor. The result is an enhanced attenuation of the through signal, with similar shunt decoupling, but also having less resonant circuit effects. These characteristics can be extremely useful to decouple very broadband nodes around both the Silicon and GaAs semiconductor devices.

Figure 2: Modeled E-Field Choke Response (including wirebonds)

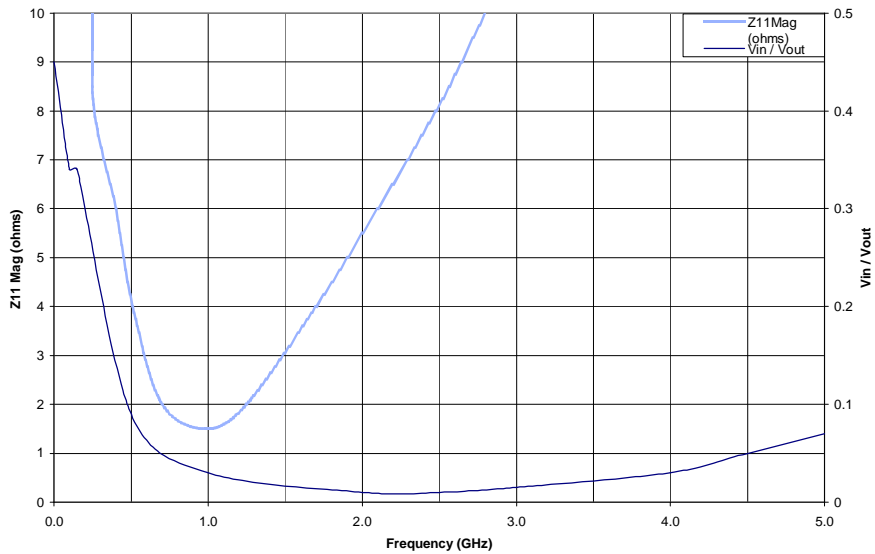
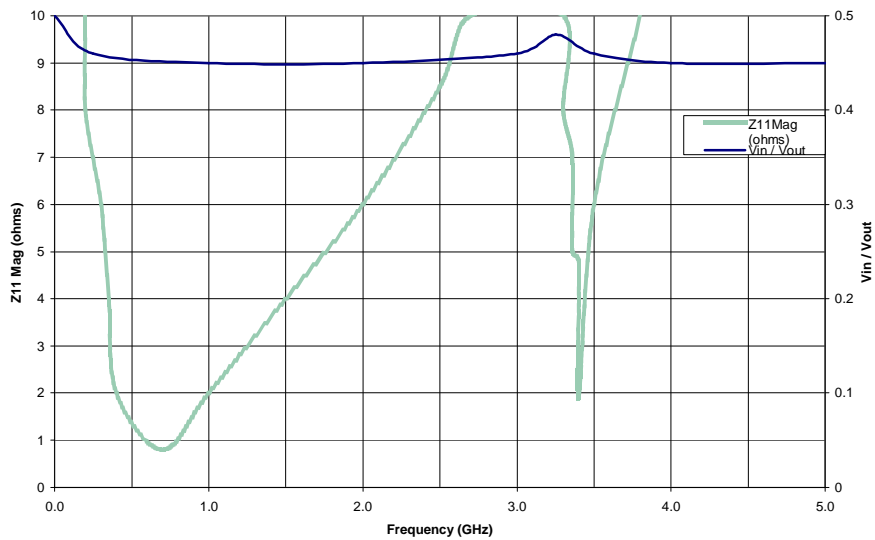


Figure 3: Modeled Capacitor Response (including wirebonds)



APPLICATION

A typical circuit application is with a mixed signal IC where an analog waveform is generated, with timing and control logic on the same IC. The analog portion of the chip has the need for external voltage references which establish absolute output voltage accuracy. These interfaces are considered "DC" but they are intimately coupled to internal high speed circuitry. Due to less than perfect internal circuit elements and internal isolation of the semiconductor, noise currents are developed at these input/output nodes. The flow of these currents through the external decoupling circuit elements and their respective parasitics will superimpose noise voltage on the nominal voltage reference, which in turn may modulate the output high performance signal. This results in signal integrity reduction, increasing system generated noise and general distortion of the desired waveform.

In the real world of mixed signal devices, a device having 0.5 to 1.0 nsec internal or external rise/fall times will typically have amplitude noise modulated currents with a period ranging from approximately 1.0 nsec (1.0 GHz fundamental frequency) to 500 psec (2.0 GHz fundamental frequency). These signals "leak out" on the nominal DC pins. The currents in a well designed IC could be up to 100 μ A peak and have significant components beyond the second harmonic of the fundamental frequencies or 4.0 GHz.

DECOUPLING OPTIONS

1. Large external decoupling capacitor

The first solution option is usually the use of the biggest capacitor which will fit as close to the IC as possible. That is defined as a capacitor with nearly zero ohms reactance. This is not the best solution since at these periods (frequencies) the inductance of the connection from the chip through the package to the capacitor has a large inductive reactance and long physical length relative to the frequencies of concern. This static inductance for packaged devices can be on the order of 5 to 10nH. The reactance for this inductance is in excess of 30 to 60 ohms at the fundamental or 60 to 120 ohms at the harmonic frequencies, assuming no "distributed" effects. The actual high frequency inductance is much higher because of the "distributed effects" of physical length. The impedance levels allow noise voltages to be developed on the voltage reference pins of up to 12 mV without the distributed effects and significantly higher with them.

2. Small decoupling capacitor next to the IC

A better solution is a parallel plate capacitor having equal reactance to the bond wire inductance and resonance for an effective inductance of zero ohms. This would be ideal for single frequency noise or extraneous signals. The major drawback is that noise is not single frequency but a range, for this example it spans 1.0 to 4.0 GHz, and it is difficult to have a broad band resonance with a single capacitor.

3. Decoupling with a CRC element

This approaches the optimum. The smaller capacitance input and output segments effectively resonate with bond wires at the higher frequency and the series resistor absorbs the noise power of the lower frequency. There is a trade-off involved. Higher series resistance affects lower frequency decoupling efficiency of any external capacitors.

4. Decoupling with an E-Field Choke

An E-Field ChokeTM incorporates another circuit element to improve the performance of CRC networks. In the E-Field ChokeTM the resistance versus frequency is enhanced so that higher frequency components are attenuated more than the lower frequency. This means series resistance (DC) is reduced to allow better low frequency decoupling while shunt capacitance is designed to be optimal for higher frequency components.

OTHER APPLICATION

The E-Field ChokeTM is a four contact device, in addition to the backside ground. The availability of these other contacts offers flexibility for application. Figure 4 shows the four top surface contacts. Alternate bonding schemes still benefit from the enhanced through isolation and "resonance-free" bypass characteristics, as shown in Figure 6 (see page 6).

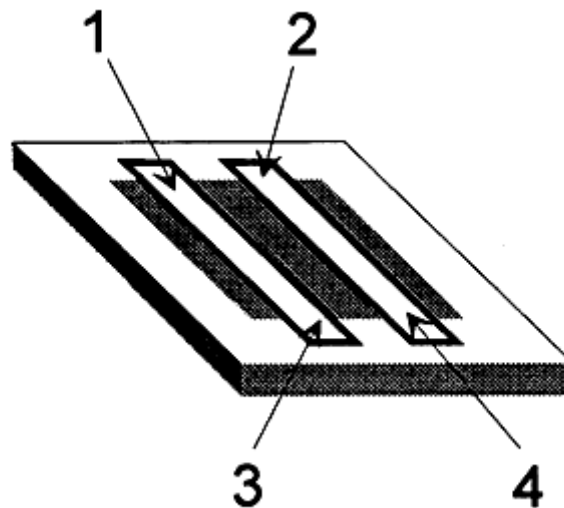


Figure 4 Top Surface Contacts

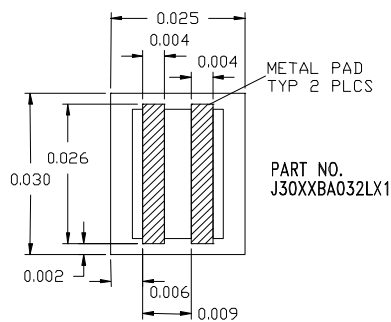
SPECIFICATION

E-Field Choke part numbering is, using J30BHBA002LX3 as an example:

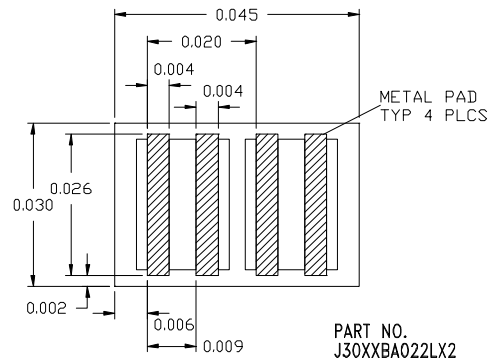
J	an RC network product
30	substrate width of 30 mils
BH	temperature coefficient of capacitance of $\pm 15\%$
B	medium impedance design
A00	unique drawing reference
2	25 VDC voltage rating
L	metalization of Ta ₂ N-TiW-Au/TiW-Au
X	commercial test level
3	number of RC units on the substrate (bar-cap style)

Four standard designs exist, from one to four pads with a nominal thickness of 7 mils:

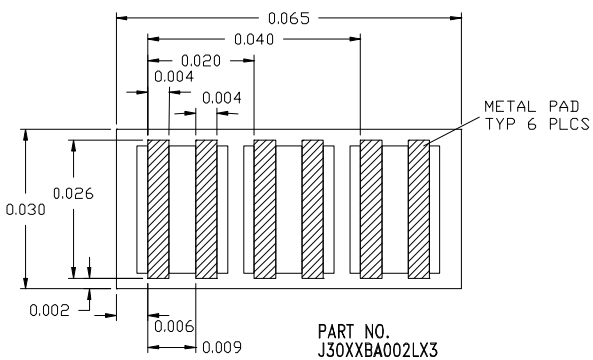
J30BHBA032LX1 (One RC "unit", 25 x 30 mils)



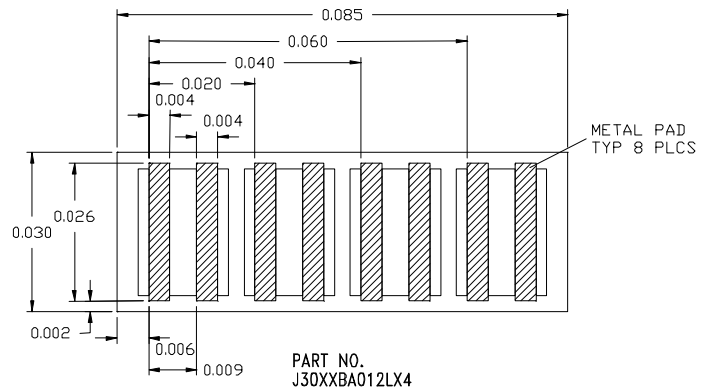
J30BHBA022LX2 (Two RC "unit", 45 x 30 mils)



J30BHBA002LX3 (Three RC "unit", 65 x 30 mils)



J30BHBA012LX4 (Four RC "unit", 85 x 30 mils)



Gold is 100 micro inches minimum of fully sputtered pure gold. Backside metalization is capable of gold eutectic or epoxy die attach. The top pattern, each RC unit, has two gold bonding stripes overlapping resistive metal (Ta_2N).

The capacitance of each top pattern is nominally 38 pF, measured at 1 MHz and room temperature. The DC resistance from stripe to stripe is nominally 10 ohms. The top-to-bottom insulation resistance of each unit is 10^5 megohms minimum at rated voltage and room temperature. The top-to-bottom dissipation factor of each unit is 2.5% maximum, measured at 1 MHz and 0.2 volts. The voltage rating of commonly 25 volts but higher ratings are possible. The stripe-to-stripe current rating of each unit is 40 mA DC by design but is not tested.

The commercial test code means a 1% AQL, level II, test for capacitance, IR, stripe-to-stripe resistance, and DWV. Visual inspection is "four-sided" using DLI bar-cap[®] criteria.

Network analyzer testing is only done to confirm the design. Testing is done on open-circuited configurations (microstrip-to-stripe stripe-to-microstrip bonding, with no bonded terminations on the opposite stripe ends). Actual scalar network analyzer sweeps are given, see figures 5a, 5b, 6, and 7.

Figures 5a and 5b "Normal" bonding (as shown):

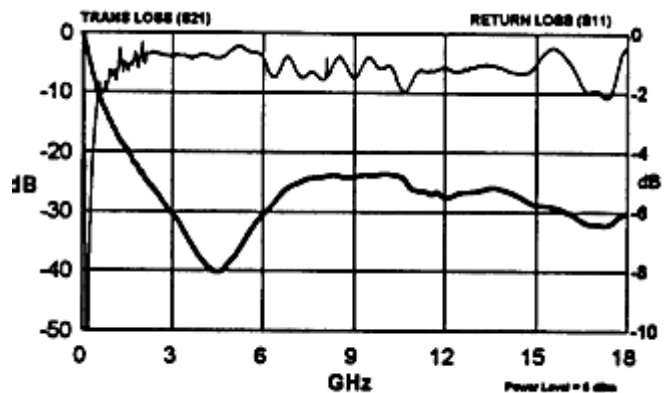


Figure 5a

Figure 5b's graph scale is changed to highlight the 1 to 5 GHz bypass benefit discussed in the APPLICATION section above.

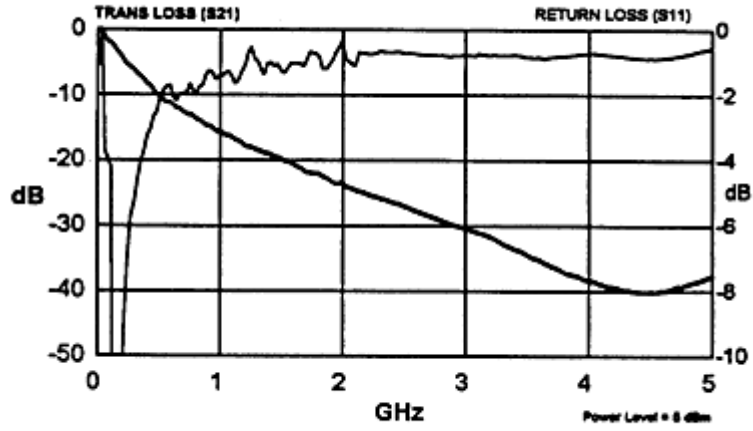


Figure 5b

Figure 6 “Same stripe” bonding:

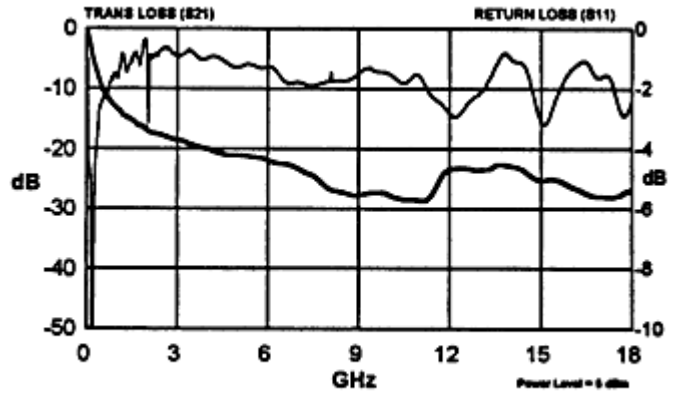


Figure 7 Bonded from one unit to the next on a multi-pad E-field Choke:

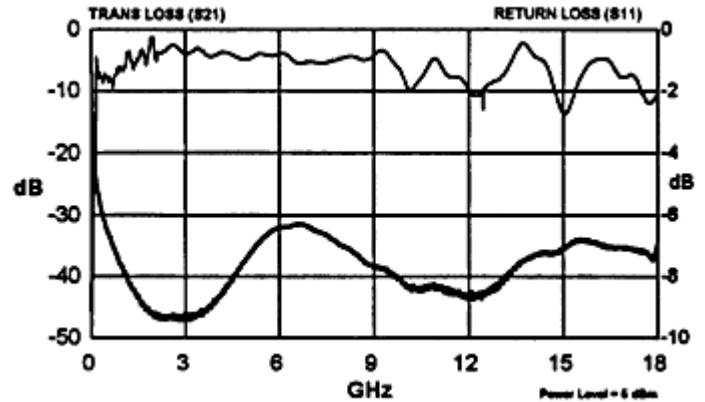


Figure 7 shows the RF isolation, unit-to-unit, of a multipad E-Field Choke™

CONCLUSION

Demanding more robust performance from today's semiconductor ICs makes the job of effectively decoupling sensitive voltage reference input/output nodes more difficult. The needs of broadband decoupling can be best met with the use of sophisticated transmission line based conductor-resistor networks on high dielectric constant material. The Dielectric Laboratories' E-Field Choke CRC networks are the components designed and manufactured to meet these needs. Please call us if you have any questions.



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