

Chip Selection

Multilayer capacitors (MLC) are categorized by dielectric performance with temperature, or “temperature coefficient”, as these devices vary in behavior over temperature. The choice of component is thus largely determined by the temperature stability required of the device, i.e. type of dielectric, and the size necessary for a given capacitance and voltage rating. The following items are pertinent to chip selection:

Dielectric Type

CF: Ultra stable Class I dielectric exceeds EIA COG requirements with negligible dependence of electrical properties on temperature, voltage, frequency and time, used in circuitry requiring very stable performance.

AH: EIA Class 1 dielectric with a dielectric constant that increases with temperature (90ppm/°C). Useful for temperature compensation where other board components may be losing capacitance with temperature.

NA: EIA Class 1 dielectric with a negative TCC. Useful in situations where other board components are gaining capacitance with temperature.

UL: EIA Stable Class 1 dielectric, with extremely low ESR. Useful in any application where heat generation or signal loss are concerns.

BL: EIA Stable Class II dielectric (X7R), with predictable change in properties with temperature, voltage, frequency and time. Used as blocking, de-coupling, bypassing and frequency discriminating elements. This dielectric is ferroelectric, and provides higher capacitance than Class 1.

MS: Stable Class 1 dielectric. Particularly suited to high capacitance or high volume applications.

Capacitor Size

Size selection is based primarily on capacitance value, voltage rating, and resonance frequency. Smaller units are generally less expensive; 0603 is the most economical size. Because mass affects the thermal shock behavior of chips, size selection must consider the soldering method used to attach the chip to the board. C18 and smaller can be wave, vapor phase or reflow soldered. Larger units require reflow soldering.

Termination Material

Nickel barrier termination, with exceptional solder leach resistance is recommended for all applications involving solder. DLI offers two versions of the nickel barrier termination. The “Z” termination is a nickel barrier with 100% matte tin for a lead free capacitor. The “U” termination is a nickel barrier with 90/10 tin/lead for military applications. Non-magnetic versions of these termination finishes are also available.

Solder Leaching

DLI’s termination finishes are designed to withstand RoHS attachment methods. During soldering, time above 230°C should be minimized to reduce thinning of the barrier layer and subsequent bond failure. DLI offers enhanced magnetic and non-magnetic termination finishes for applications requiring extended soldering time or repeated reflow cycles. Please consult your Sales Representative when ordering.

Packaging

Units are available in bulk, reeled or in waffle pack.

Attachment Methods

Bonding of capacitors to substrates can be categorized into two methods, those involving solder, which are prevalent, and those using other materials, such as epoxies and thermo-compression or ultrasonic bonding with wire. Please see DLI application note “Recommended Solder Attachment Techniques for Multi-Layer Chip and Pre-Thinned Capacitors” located on our website, www.dilabs.com.

Soldering

Soldering methods commonly used in the industry and recommended are Reflow Soldering, Wave Soldering, and to a lesser extent, Vapor Phase Soldering. All these methods involve thermal cycling of the components and therefore the rate of heating and cooling must be controlled to preclude thermal shocking of the devices. In general, rates which do not exceed 120°C per minute and a temperature spike of 100°C maximum for any soldering process on sizes C18 and smaller is advisable. Other precautions include post soldering handling, primarily avoidance of rapid cooling with contact with heat sinks, such as conveyors or cleaning solutions.

Large chips are more prone to thermal shock as their greater bulk will result in sharper thermal gradients within the device during thermal cycling. Units larger than C18 experience excessive stress if processed through the fast cycles typical of solder wave or vapor phase operations. Solder reflow is most applicable to the larger chips as the rates of heating and cooling can be slowed within safe limits. In general, rates that do not exceed 60°C per minute and a temperature spike of 50°C maximum for any soldering process on sizes larger than C18 is advisable.

Attachment using a soldering iron requires extra care, particularly with large components, as thermal gradients are not easily controlled and may cause cracking of the chip. Precautions include preheating of the assembly to within 100°C of the solder flow temperature, the use of a fine tip iron which does not exceed 30 watts, and limitation of contact of the iron to the circuit pad areas only.

Bonding

Hybrid assembly using conductive epoxy or wire bonding requires the use of silver palladium or gold terminations. Nickel barrier termination is not practical in these applications, as intermetallics will form between the dissimilar metals. The ESR will increase over time and may eventually break contact when exposed to temperature cycling.

Cleaning

Chip capacitors can withstand common agents such as water, alcohol and degreaser solvents used for cleaning boards. Ascertain that no flux residues are left on the chip surfaces as these diminish electrical performance.

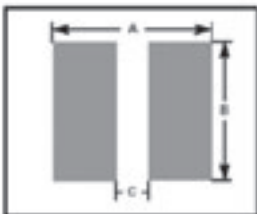
DLI Shelf Life

Capacitors are solderable for a maximum of one year from the date of shipment if properly stored in the original packaging. Dry nitrogen storage is preferable for longer periods.

Board Design Considerations

The amount of solder applied to the chip capacitor will influence the reliability of the device. Excessive solder can create thermal and tensile stresses on the component which could lead to fracturing of the chip or the solder joint itself. Insufficient or uneven solder application can result in weak bonds, rotation of the device off line or lifting of one terminal off the pad (tombstoning). The volume of solder is process and board pad size dependent. WAVE SOLDERING exposes the devices to a large solder volume, hence the pad size area must be restricted to accept an amount of solder which is not detrimental to the chip size utilized. Typically the pad width is 66% of the component width, and the length is .030" (.760 mm) longer than the termination band on the chip. An 0805 chip which is .050" wide and has a .020" termination band therefore requires a pad .033" wide by .050" in length. Opposing pads should be identical in size to preclude uneven solder fillets and mismatched surface tension forces which can misalign the device. It is preferred that the pad layout results in alignment of the long axis of the chips at right angles to the solder wave, to promote even wetting of all terminals. Orientation of components in line with the board travel direction may require dual waves with solder turbulence to preclude cold solder joints on the trailing terminals of the devices, as these are blocked from full exposure to the solder by the body of the capacitor. Restrictions in chip alignment do not apply to SOLDER REFLOW or VAPOR PHASE processes, where the solder volume is controlled by the solder paste deposition on the circuit pads. There are practical limitations on capacitor sizes that prohibit reliable direct mounting of chip capacitors larger than 2225 to a substrate. Without mechanical restriction, thermally induced stresses are released once the capacitor attains a steady state condition, at any given temperature. Capacitors bonded to substrates, however, will retain some stress, due primarily to the mismatch of expansion of the component to the substrate; the residual stress on the chip is also influenced by the ductility and hence the ability of the bonding medium to relieve the stress. Unfortunately, the thermal expansions of chip capacitors differ significantly from those of substrate materials.

Recommended Printed Wire Board Land Patterns



Printed Wire Board land pattern design for chip components is critical to ensure a reliable solder fillet, and to reduce nuisance type manufacturing problems such as component swimming and tombstoning. The land pattern suggested can be used for reflow and wave solder operations as noted. Land patterns constructed with these dimensions will yield optimized solder fillet formation and thus reduce the possibility of early failure.¹

$$A = (\text{Max Length}) + 0.030" (.762\text{mm})^*$$

$$B = (\text{Max Width}) + 0.010" (.254\text{mm})^{**}$$

$$C = (\text{Min Length}) - 2 (\text{Nominal Band})^{***}$$

* Add 0.030" for Wave Solder operations.

** Replace "Max Width" with "Max Thickness" for vertical mounting.

*** "C" to be no less than 0.02", change "A" to (Max Length) + 0.020". For C04 "C" to be no less than 0.01".

1. Frances Classon, James Root, Martin Marietta Orlando Aerospace, "Electronics Packaging and Interconnection Handbook".

Temperature Precautions

The rate of heating and cooling must be controlled to preclude thermal cracking of ceramic capacitors. Soldering temperatures should not exceed 200°C per minute, temperature variation must not exceed 100°C maximum for any solder operation. Avoid forced cooling or contact with heat sinks, such as conveyor belts, metal tables or cleaning solutions, before the chips reach ambient temperatures.

MLC Orientation - Horizontal and Vertical Mounting

The orientation of the MLC relative to the ground plane affects the devices' impedance. When the internal electrodes are parallel to the ground plane (Horizontal mounting) the impedance of the MLC resembles a folded transmission line driven from one end. The below graph shows the modeled insertion loss and parallel resonances of C17AH101K-7UN-X0T with horizontal mounting. When the internal electrodes are perpendicular to the ground plane (Vertical mounting, bottom graph) the MLC impedance resembles a folded transmission line driven from the center reducing resonance effects. C11,17 are available with vertical or horizontal orientation in tape and reel packaging. Modeling can be done in CapCad. HP/EEs of series 4 contains models for C11 and C17 in the element libraries under Dielectric Laboratories MLC.

